Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 10608 - 10619
Received 25 April 2021; Accepted 08 May 2021.

Current programmed transfer function model of Luo Converters for Standalone Photovoltaic System

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ABSTRACT

This paper proposes a new transfer function model known as current programmed transfer function model of Luo converter for standalone photovoltaic system. This model eliminates the need of current loop for regulating load current and helps in achieving perfect current sharing in paralleled connected converter modules. Thus the control strategy of paralleled connected Luo converters consists of only one voltage loop. This voltage loop generates a control signal which is influenced by the inaccuracy that occurs in output voltage. The control signal is given as input to current programmed transfer function model of Luo converter. This ensures identical distribution of load current among paralleled connected converters. The proposed system reduces system complexity by eliminating the need of separate current loop. The outcomes of simulations are offered to confirm that the suggested scheme is possible.

Keywords
PV array, PSLLC, Parameter mismatches, current loop, voltage loop

1.Introduction

In latest years, photovoltaic (PV) schemes have been used to harness the sun's energy for generating power. Sunlight is openly transformed to electricity by a PV device. To progress the power from the PV unit, utmost applications need electronic converters [1-4]. Since the characteristics of solar cells are not linear, it is important to run a PV array as efficiently as possible. A maximum power point monitoring method using ANFIS is suggested to make certain extreme performance.

In the electricity production, creating more power is vital. More output power is produced when more number of low power converters are used in parallel. For generating more current, Luo converters joined in parallel with solar input are used in this article. In this case current at the output not distributed evenly among converters. As a result, a new current division system for identical load current distribution is proposed.

For even division of current through load, there are a variety of current distribution schemes available. The droop technique [5]- [6] is one of the most widely used techniques for providing stable operation in converters linked in parallel. Load sharing is reliant on output-voltage control, which is a disadvantage of this system.

Active current-division structures are another current-division structure [7–11]. As an input to the control loop, the change in values among the reference current and the current at the output of each converter module is given.The master–slave regulator is a popular current-sharing approach, where all slave units obey the master's reference present.

[12] Offered a control structure for distributing current. Separate loops were used for voltage (output) and current (inner). DSP was used to enforce the regulating structure. The loop for current needs a regulator for regulating current, where duty ratio is fine-tuning directly.

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To distribute current evenly, a control structure with three-loops were used surges circuit complication.[14] Introduced multi-ring control arrangement with a duty cycle that is static and common. [15] Suggested a popular duty ratio control structure converters that are joined at source and load in parallel.

Converters (with half wave rectifiers) linked in parallel at output use a regular duty ratio control structure to segment current [16]. In [17], a interleaving link in the rectifier diodes was utilized to mechanically distribute currents in two half-bridge converters.

A current division regulator is required in [12] and [13], which surges circuit complication. However, current distribution happens in [14] to [17] based on standard duty ratio. The disadvantage is that if there are more components misalliances among converters, no exact current distribution takes place.This article presents current distribution without using a particular current regulator. Also improved current distribution occurs for more components misalliances.

In this article, an innovative control structure with a loop for regulating voltage in the external section and a loop for controlling current in the inner section is suggested. Using ANFIS, the former loop aids in getting a controlled output. Without using any regulator, the later loop conducts current distribution.The regulating structure also does not explicitly change the duty ratio of converter. The duty ratio of converters joined in parallel is fine-tuned which depends on the source at the input, current through inductor and voltage drop across capacitor.

MPPT of photovoltaic system is offered in section 2. Section 3 discourses block diagram of suggested method. Section 4 explains how to get the system function of PSLLC. ANFIS design is explained in section 5. Section 6 offers the virtual reality and results obtained through hardware. The inference is deliberated in section 7.

2. MPPT in Photovoltaic system

The Fuzzy logic controller (FLC) with constant voltage reference technique of the MPPT process is used for getting more power [18]. The signal (voltage and current) from the solar panel are sensed, as shown in Fig 1. To produce an error signal, the sensed voltage is matched to the reference voltage. The MPPT (FLC) regulator accepts this error signal as response. Based on the response, signal is produced by the MPPT regulator.

3. Block diagram of proposed system

Figure 1 depicts the suggested structure's block diagram. Solar panels, converters (buck-boost), Regulator to get more power, batteries, and PSLLCs joined in parallel that serve as load regulators are the key components.

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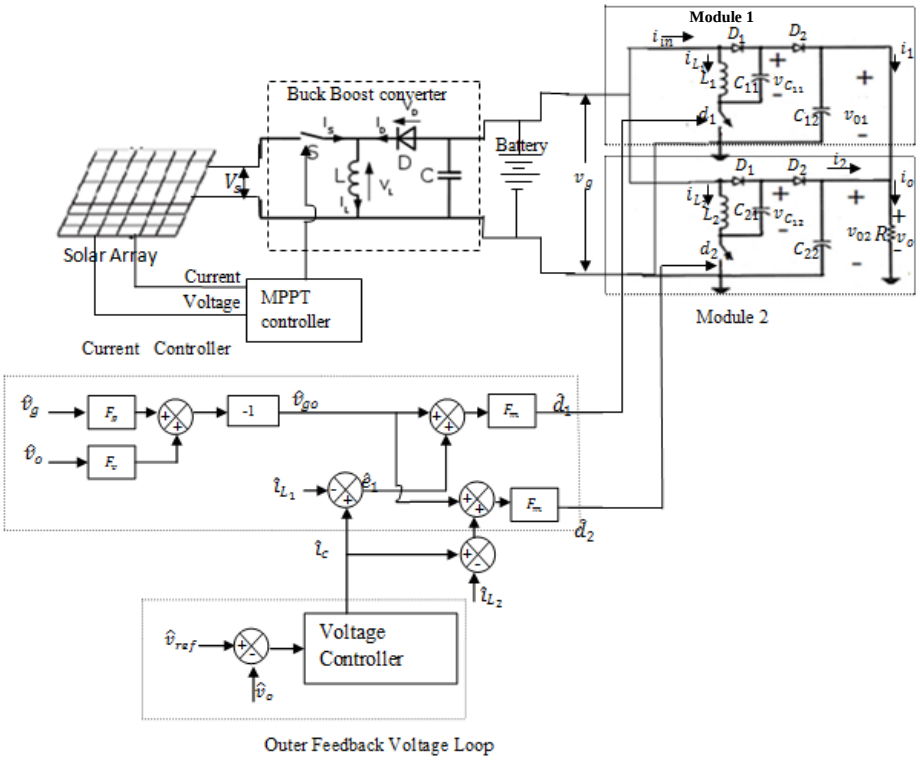

Figure 1. Block Diagram of Proposed structure

The electrical signals are sensed in the existence of radiation. FLC varies the duty ratio of the converter to achieve the wanted voltage at the output, which depends on the changeamong real and set point voltages. The battery receives the converter's output. The battery's minimal voltage is 12V. The battery in this case is a lead acid battery.

If the energy from solar group is inadequate, both battery and PV system collectively provide the necessary power to loads. If radiation is not there, the load is driven solely by the battery. When the converter detects that the battery is completely charged, the charge flow from the solar array is stopped. The load receives the production from the battery via PSLLCs.

Paralleled linked PSLLCs serve as a regulator for load in the suggested framework. To confirm a higher current at the output, two PSLLCs are joined at the source and load in parallel. If there are component misalliances, current dissimilarity occurs [19-21].

To distribute the current evenly amongconverters, a novel control structureis used which is not having a particular regulator for regulating curren. Also no direct adjustment of duty ratio takes place. Converter output depends mainly on converter input, current flows via inductor and drop across capacitor.

In the case of component misalliances, a novel control arrangement without a controller is used to distribute the load current via load uniformly among converters. The duty ratio of PSLLCs is regulated by the source, current via inductor, and voltage across capacitor.

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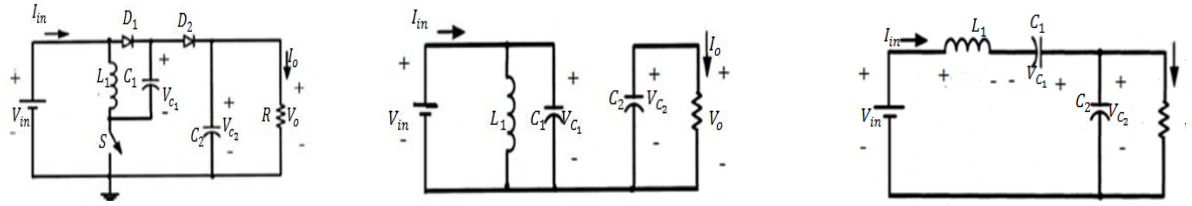
The control structure aims in regulating voltage and current. Depends on the difference between actual ($\hat{v}_o$) and reference ($\hat{v}_{ref}$) signal the loop meant for voltage produce a signal. The reference signal for current regulator is taken from voltage loop. Current regulator comprises effective feedback of the inductor currents ($\hat{\imath}_{L_1}$) and($\hat{\imath}_{L_2}$) , the outer feedback voltage (capacitor voltage ($\hat{v}_o$)) and the effective feed forward of the input voltage (power input voltage (($\hat{v}_g$)).F_g and F_v are the gains of the output voltage ($\hat{v}_o$) and the effective feed forward of the input voltage ($\hat{v}_g$) respectively.F_m is the common gain of current controller. The negative value of sum of signal from outer feedback voltage loop and the effective feed forward of the input voltage generates a signal ($\hat{v}_{go}$). The control signal ($\hat{\imath}_c$) is compared with the inductor currents ($\hat{\imath}_{L_1}$)and (i_{L_2}) of IPOP connected PSLLCs to generate an error signals (($\hat{e}_1$) and ($\hat{e}_2$)). These error signals gets added with the signal ($\hat{v}_{go}$) to generate a control signal which adjusts the duty ratio of IPOP connected PSLLCs. This ensures even distribution of current flowing through load.

4. System Function of PSLLC (Direct)

The circuit of PSLLC is depicted in Figure2[22].



(a) Circuit of PSLLC (b) Mode 1 Operation of PSLLC (c) Mode 2 Operation of PSLLC

Figure 2. Circuit of PSLLC and its different modes of operation

The source of the circuit is V_{in}, once supply is given, the switch gets closed and open and as a result,

The expression for current flowing through inductor is

$$L\frac{d\hat{\imath}(t)}{dt} = \hat{v}_g(t) + D'\left(\hat{v}_1(t) - \hat{v}_2(t)\right) - \hat{d}(t)(V_1 - V_2) \quad (1)$$

Similarly the voltage drops across capacitor is

$$C_1\frac{d\hat{v}_1(t)}{dt} = -D\hat{\imath}_{L_1}(t) - \hat{d}(t)I_{L_1} + \hat{\imath}_{in}(t) \quad (2)$$

$$C_2\frac{d\hat{v}_2(t)}{dt} = -\frac{\hat{v}_o(t)}{R} - \hat{d}(t)I_o + D'\hat{\imath}_o(t) \quad (3)$$

The expression for input current is

$$\hat{\imath}_g(t) = D\left(\hat{\imath}_{L_1}(t) + \hat{\imath}_{C_1}(t)\right) + \hat{d}(t)\left(I_{L_1} + I_{C_1} - I_{C_2} - I_o\right) + D'\left(\hat{\imath}_{C_2}(t) + \hat{\imath}_o(t)\right) \quad (4)$$

Follow-on equations 1, 2, 3 and 4 the modified circuit of PSLLC is is shown in Figure 3.

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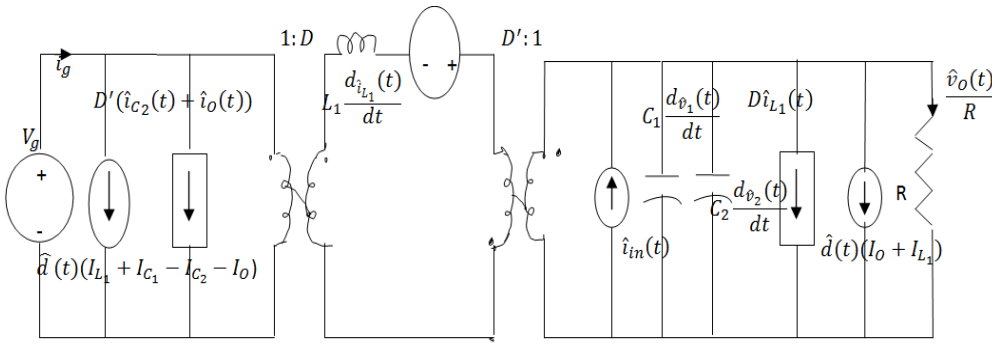

Figure 3. Small signal equivalent circuit of PSLLC

From Fig. 3. The system function considering line and load is expressed as

$$G_{V_g}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)} = \left(-\frac{D}{D'}\right)\frac{1}{1+\frac{L}{D'^2}S+\frac{RL(C_1+C_2)S^2}{D'^2}}. \quad (5)$$

$$G_{v_{\hat{d}}}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)},$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \left(-\frac{(V_1-V_2)}{D'}\right)\frac{\left[1+S\frac{LI_o}{D'(V_1-V_2)}\right]}{\left[1+\frac{L}{RD'^2}S+S^2L\left(\frac{C_1+C_2}{D'^2}\right)\right]}. \quad (6)$$

4.1 System function of PSLLC (indirect)

The averaged equations for PSLLC were given by equations 1, 2, 3 and 4. Applying laplace to equation 1 the linearised inductor equation is

$$SL\hat{\imath}_{L_1}(s) = \hat{v}_g(s) + D'\left(\hat{v}_1(s) - \hat{v}_2(s)\right) - \hat{d}(s)(V_1 - V_2) \quad (7)$$

Similarly applying laplace to equations 2 and 3 the linearised capacitor equations are

$$SC_1\hat{v}_1(s) = -D\hat{\imath}_{L_1}(s) - \hat{d}(t)I_{L_1} + \hat{\imath}_{in}(s) \quad (8)$$

$$SC_2\hat{v}_2(s) = -\frac{\hat{v}_o(s)}{R} - \hat{d}(s)I_o + D'\hat{\imath}_o(s) \quad (9)$$

The linearised average input current is

$$\hat{\imath}_g(s) = D\left(\hat{\imath}_{L_1}(s) + \hat{\imath}_{C_1}(s)\right) + \hat{d}(s)\left(I_{L_1} + I_{C_1} - I_{C_2} - I_o\right) + D'(\hat{\imath}_{C_2}(s) + \hat{\imath}_o(s)) \quad (10)$$

Assume $\hat{\imath}_{L_1}(s) = \hat{\imath}_{c_1}(s)$

From equation (7)

$$SL\hat{\imath}_{c_1}(s) = \hat{v}_g(s) + D'\left(\hat{v}_1(s) - \hat{v}_2(s)\right) - \hat{d}(s)(V_1 - V_2) \quad (11)$$

Therefore

$$\hat{d}(s) = \frac{\hat{v}_g(s) + D'\left(\hat{v}_1(s) - \hat{v}_2(s)\right) - SL\hat{\imath}_{c_1}(s)}{(V_1 - V_2)} \quad (12)$$

From equation (8)

$$SC_1\hat{v}_1(s) = -D\hat{\imath}_{c_1}(s) - \hat{d}(t)I_{L_1} + \hat{\imath}_{in}(s) \quad (13)$$

$$SC_1\hat{v}_1(s) = -D\hat{\imath}_{c_1}(s) + \hat{\imath}_{in}(s) - I_{L_1}\frac{\hat{v}_g(s) + D'\left(\hat{v}_1(s) - \hat{v}_2(s)\right) - SL\hat{\imath}_{c_1}(s)}{(V_1 - V_2)} \quad (14)$$

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From equation (9)

$$SC_2\hat{v}_2(s) = -\frac{\hat{v}_o(s)}{R} + D^{'}\hat{\imath}_o(s) - I_o\frac{\hat{v}_g(s)+D^{'}(\hat{v}_1(s)-\hat{v}_2(s))-SL\hat{\imath}_{c_1}(s)}{(V_1-V_2)} \quad (15)$$

From equation (10)

$$\hat{\imath}_g(s) = D\left(\hat{\imath}_{L_1}(s)+\hat{\imath}_{C_1}(s)\right) + \left(I_{L_1}+I_{C_1}-I_{C_2}-I_o\right)\frac{\hat{v}_g(s)+D^{'}(\hat{v}_1(s)-\hat{v}_2(s))-SL\hat{\imath}_{c_1}(s)}{(V_1-V_2)} + D^{'}(\hat{\imath}_{C_2}(s)+\hat{\imath}_o(s)) \quad (16)$$

Assuming $V_1 = V_g$ and $V_2 = V$,$V = -\frac{D}{D^{'}}V_g$ and $I_L = -\frac{V}{D^{'}R}$, Circuit modeled based on above equations is shown in Figure 4

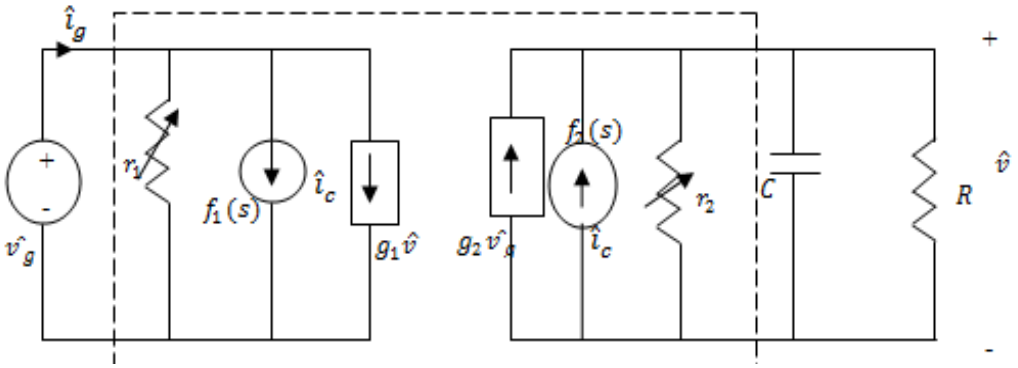

Figure 4. Two port equivalent circuit to model current programmed PSLLC

From Figure 4 the transfer function by setting v_g to zero is

$$G_{V_c}(s) = -D^{'}\left(1-\frac{SDL}{D^{'2}R}\right)\left[\frac{R}{D}parallel\ R\ parallel\ \frac{1}{SC}\right] \quad (17)$$

$$G_{V_c}(s) = \frac{\hat{v}(s)}{\hat{\imath}_c(s)} \quad (18)$$

$$G_{V_c}(s) = R\frac{D^{'}}{1+D}\frac{1-S\frac{DL}{D^{'2}R}}{1+\frac{SRC}{1+D}} \quad (19)$$

By setting $\hat{\imath}_c$ to zero , the equivalent expression is

$$G_{V_g}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)} \quad (20)$$

$$G_{V_g}(s) = -\frac{D^2}{D^{'}R}\left(\frac{R}{D}\text{ parallel R parallel }\frac{1}{SC}\right) \quad (21)$$

$$G_{V_g}(s) = -\frac{D^2}{D^{'}R}\left(\frac{1}{1+\frac{SRC}{1+D}}\right) \quad (22)$$

Equations (19) and (22) express the system function of PSLLC

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5 ANFIS Model for Paralleled connected PSLLCs

In ANFIS modelling input-output data pairs from converter modules are considered. In the dataset, the source is the change in actual and set point voltage and the output y(t) is the control signal for inner current regulator.

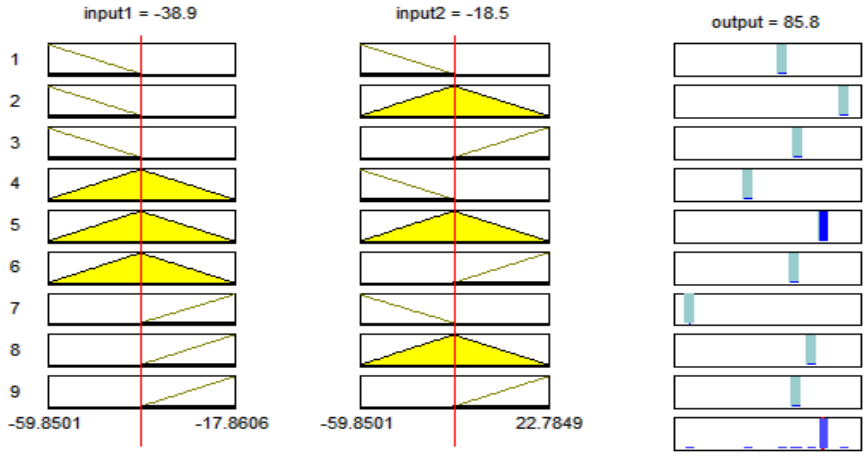

Figure 5. ANFIS rules for regulating load voltage

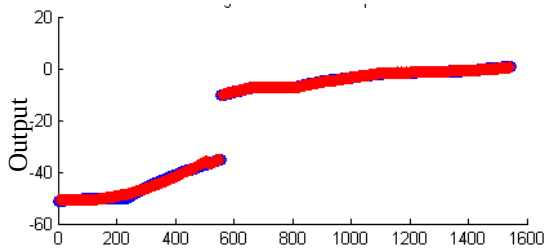

Figure 6. Actual output and the output predicted by the ANFIS

ANFIS rules, actual and predicted output and training error are shown in Fig. 5, 6 and 7 respectively.

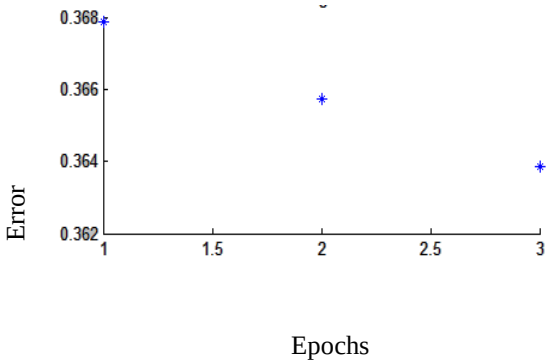

Figure 7. Training error of the ANFIS model

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The diagrammatic representation of PSLLC with ANFIS is shown in Figure 8.The signal from ANFIS depends on error '$e(k)$' and change in error $\Delta e(k)$ and are expressed as

$$e(k) = V_{ref} - V_0, \quad (23)$$

$$\Delta e(k) = e(k) - e(k-1). \quad (24)$$

Where V_{ref} is the set-point voltage and V_o is the real output voltage of PSLLC. The signal from FLC is nothing but, the modification in duty ratio Δd.

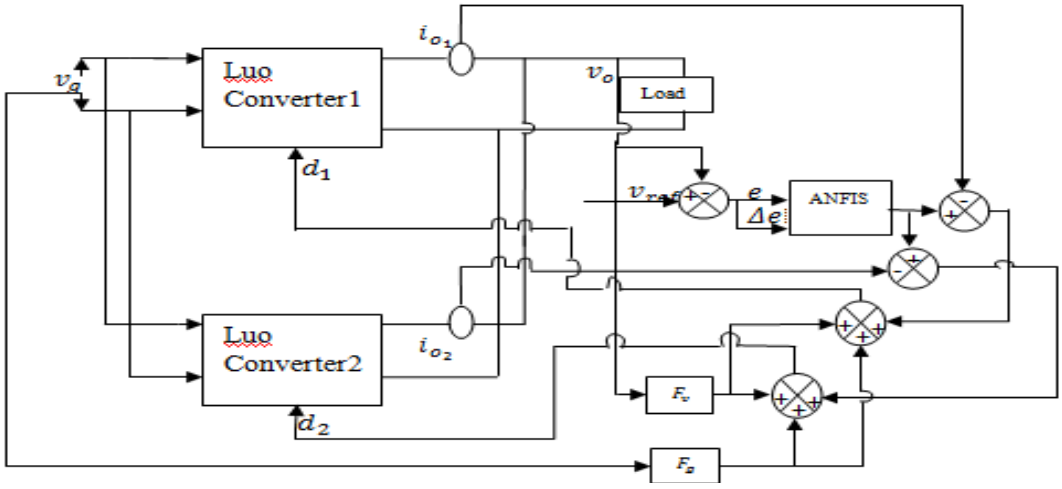

Figure 8. Block Diagram of Proposed System with ANFIS

The signal from ANFIS acts as a set-point signal for current regulator. Current regulator regulate the duty cycle of particular converter based on the current via inductor, voltage across capacitor and input source to share the current uniformly between two paralleled connected PSLLCs

6 . Results and Discussions

A stand-alone PV system is used to test the possibility of the suggested method. BPSX150 PV module is adopted as the PV array model. Paralleled connected PSLLCs is acting as a load regulator. Itis the interface among converter and the load to obtain the regulated output.

6.1 Simulation Results

Simulations are performed on PSLLCs circuits with supply of 12V and load voltage of 36V. Initially, virtual results were attained for existing and suggested technique. Figure 9 indicates that oscillation is more for existing technique.Instead of oscillation, the response of the PSLLC settles faster with the proposed method. As a result, for current sharing in PSLLCs linked in parallel, regulating duty ratio indirectly is favored.

Figure 10 shows simulation waveforms with $C_{11} = 30\mu F$ *and* $C_{12} = 35\mu F$. Figure 10 (a) shows the reaction of output voltage. The peak overshoot is 38% for ANFIS and 38.05 % for PID controller. The responses settle down at 36V for ANFIS and at 36.04V for PID controller.

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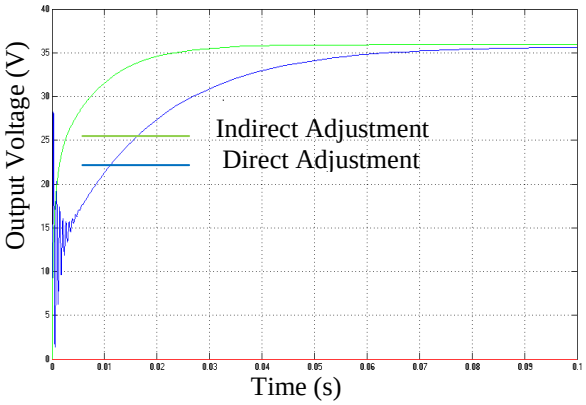

Figure 9. Comparison results for transfer function of PSLLCs with direct adjustment and indirect adjustment of duty ratio

Figure 10 (b) shows the load current, which has a little overshoot of 0.76% and 0.761% and a peak time of 0.01s both for ANFIS and PID controller. The output current is 0.72A and 0.7208A for ANFIS and PID controller respectively.
Figure 10(c) depicts current 1 which has a overshoot of 0.38% and 0.3805% for ANFIS and PID controller respectively. The output current of module 1is 0.36A for ANFIS and 0.3604A for PID controller.
Figure 10(d) demonstrates current 2 that has a overshoot of 0.38% and 0.3805% and a settle down time of 0.0125s and 0.0325s for ANFIS and PID regulator correspondingly.

Figure 10(a),(b),(c),(d) indicates exact current distribution for both ANFIS and PID controller. But the reaction is improved for ANFIS than PID controller.

Figure 11 shows simulation waveforms with $L_1 = 100\mu H \ and \ L_2 = 102\mu H$. Figure.12(a),(b) depicts current 1 and current 2 of PSLLCs linked in parallel for variation in load.It indicates that current 1 and current 2 has a overshoot and a settle down time of 0.0125s and 0.0325s for ANFIS and PID controller correspondingly.

From result it is obvious that ANFIS settle down quicker than PID regulator. Moreover ANFIS gives improved performance than PID regulator for load change.Figure 12 shows simulation waveforms with $C_{11} = 30\mu F \ and \ C_{12} = 35\mu F$ .Figure 13(a) presents the reaction of the current 1 for various load. It was observed that the maximum overshoot is 0.478%,0.38% and 0.315% for 40 Ω,50 Ω and 60 Ω correspondingly and a slow down time is 0.0125s.
Figure 13 (b) shows the reaction of current 2 for various loads with ANFIS. The reaction shows overshoot of 0.478%, 0.38% and 0.315% for 40 Ω,50 Ω and 60 Ω correspondingly and a settle down of 0.0125s.

Figure 13 (a) and (b) indicates that ANFIS regulator works well for various loads and settle down at 0.0125s.Table 3 shows the performance assessment of IPOP connected PSLLCs with ANFIS and PID controller. It indicates that performance of ANFIS is better than PID controller

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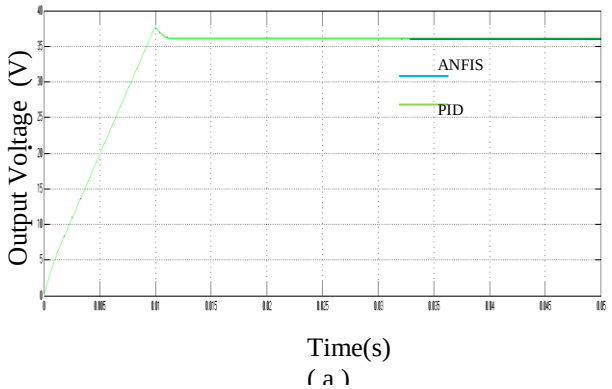
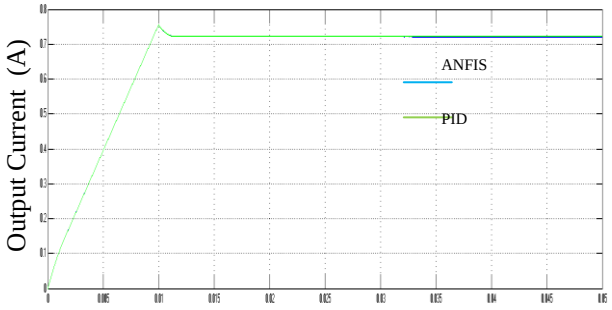
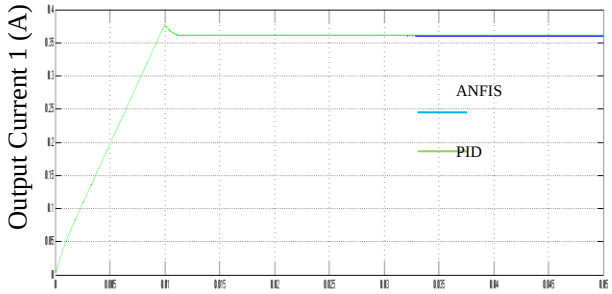


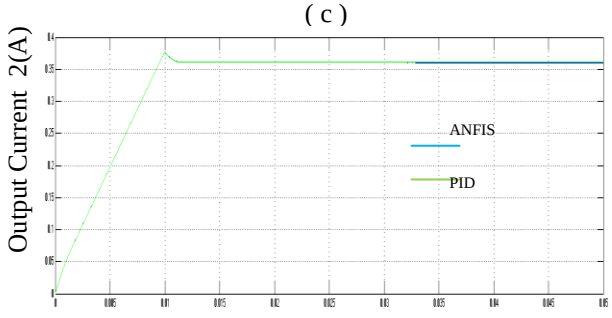
(a)



(b)

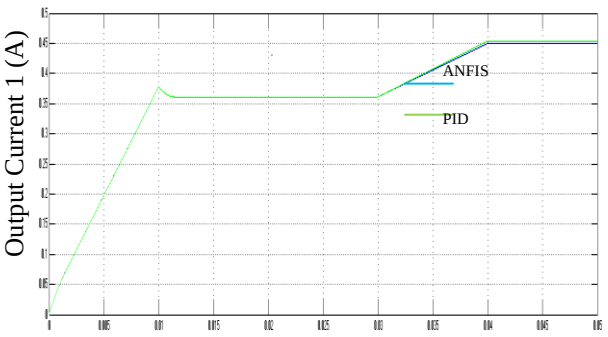


(c)

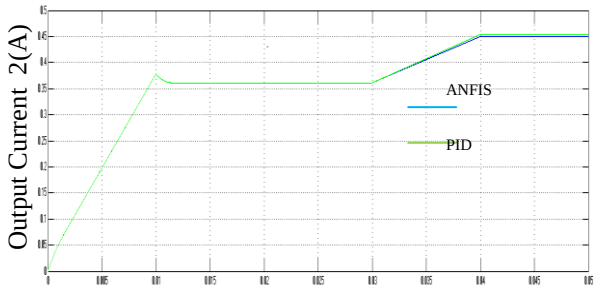


(d)

Figure 10. Simulation waveforms with $C_{11} = 30\mu F \; and \; C_{12} = 35\mu F$
(a). Output voltage for R=50Ω
(b). Current through load of 50Ω
(c). Current1 for R=50Ω
(d). Current 2 for R=50Ω

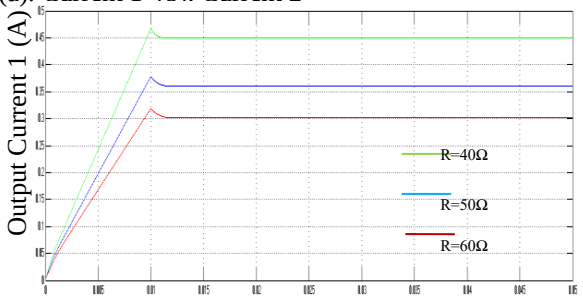


(a)

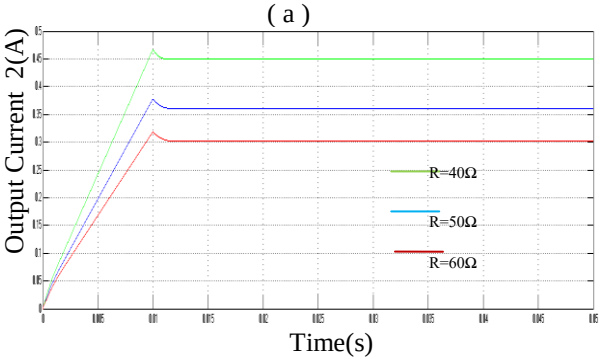


(b)

Figure 11. Simulation waveforms with $L_1 = 100\mu H \; and \; L_2 = 102\mu H$ for modification in load
(a). Current 1 (b). Current 2



(a)



(b)

Figure 12. Simulation waveforms with $C_{11} = 30\mu F \; and \; C_{12} = 35\mu F$
(a). Current 1 for several loads
(b) Current 2 for several loads

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 10608 - 10619
Received 25 April 2021; Accepted 08 May 2021.

Table 3. Performances of PSLLCs with FLC and Lag-Lead Compensator

Line/Load Variation	ANFIS				PID			
	V_0	I_0	I_{01}	I_{02}	V_0	I_0	I_{01}	I_{02}
(0-1000)W/m^2	36	.72	.36	.36	36.04	.7208	.3604	.3604
50Ω	36	.72	.36	.36	36.04	.7208	.3604	.3604
40Ω	36	0.9	.45	.45	36.04	0.901	.4505	.4505
60Ω	36	0.6	0.3	0.3	36.04	0.6	0.3	0.3

7. Conclusion

This article has offered an innovative control structure for distributing current uniformly in PSLLCs joined in parallel with solar input. To get utmost power from PV structure, FLC was used. With no particular regulator for distributing current evenly, the offered scheme confirms identical division of load current. This decreases complication of the system. To acquire a controlled output voltage ANFIS regulator was used. While matching presentation of ANFIS with PID regulator, it was detected that delimited output voltage was acquires using ANFIS.

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