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Design and Control of a Solar Photovoltaic Fed Asymmetric Multilevel Inverter Using Computational Intelligence

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ABSTRACT

Selective harmonic mitigation method is primarily used in the suppression of lower order harmonics. The Bee colony optimization method is used to implement a SHE technique in this paper; the reduced switch thirty-one stage inverter receives input voltage from the photovoltaic system. A stable voltage is maintained at the photovoltaic panel's output through a SEPIC converter. Grey Wolf Optimization is used to boost the efficiency of the photovoltaic system. Multi Carrier modulation method is often used to reduce the current and voltage harmonics in the inverter. Additionally, the proposed BCO method is compared with genetic algorithm based SHE method. The proposed suggested framework has been validated using Matlab simulation, and the prototype results have been validated using DSPIC30F2010 controller.

Keywords: Reduced switch Multilevel inverter,Selective harmonic Mitigation, SEPIC Converter,Multi Carrier,Bee colony optimization, MPPT algorithm, GWO algorithm, DSPIC controller.

1. Introduction

Solar-powered autonomous modular inverters have become increasingly popular in several applications in recent years. Due to implementation of power electronic devices in traditional inverters, the harmonic pollutants are more. This harmonic pollutant has a detrimental effect on the life span of electrical products. To address these harmonic problems, a multilevel inverter (MLI) is used [1]. Multilevel inverter reduces the switching stress and switching loss of the power semiconductor circuitry. The photovoltaic method is critical to modern life in the twenty-first century. However, because of innate temperature and luminescence variations, the output voltage of a photovoltaic device has higher cognitive ripples and often varies in output power. These disadvantages are overcome by using the Maximum Power Point Tracking (MPPT) process in conjunction with a suitable DC-DC converter. While the output power of a MLI is typically regulated via sinusoidal PWM(SPWM), switching loss including Total Harmonic Distortion(THD) are substantially higher when using high frequency modulation scheme. The modular SHE approach overcomes these disadvantages. Several works of published literature are reviewed below. The diode clamped multilevel inverter, the capacitor type multilevel inverter, and the cascaded H bridge inverter are the three primary types of

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multilevel inverters. Cascaded H Bridge MLI is the most commonly used of these three types due to its low volume, low switching stress and low switching losses, good electromagnetic interference capability, and high reliability. However, this CHBMLI is subdivided into symmetrical(SMLI) and asymmetrical (AMLI). The semiconductor switches used in SMLI is very large. The author of [1] addressed low component SMLI with varying input voltages; this configuration produces high-quality voltage level with a small number of switches. However, modulation at a high frequency tends to increase the losses.The researcher addressed the multi-stage inverter with carrier based PWM control methods in [2]. This strategy decreases the harmonic distortions but is only useful for smaller systems. The authors in [3] presented a switched capacitor MLI in which there is a reduction in the DC supplies. However, in this case, the use of capacitance creates voltage unbalance. The disadvantages of high frequency modulation are resolved using the SHE technique [4]. However, this inverter is incompatible with nonlinear loads.

2. Literature Review

Switched rectifier line voltage includes massive capacitor bank and supply from the grid. These disadvantages are resolved by [5], implementing a cascaded MLI based on photovoltaics [5]. However, the PWM employed in this article is carrier based PWM. These strategies limit the inverter's potential applications. In [6] a boost inverter is presented. However, this configuration has a large number of switches and a complex control circuit.

The paper [8] analyses a photovoltaic-based T-shape inverter. This inverter is ideal for grid-connected photovoltaic applications. The authors in [9] implement a MLI with SHE PWM using current source rectifiers. However, a rectifier that uses a current source degrades the efficiency of the input source current and raises the power loss. In [10] the author discusses the general strategies for removal of harmonics using SHE. This method would be extremely beneficial in the creation of modular or developed SHE strategies. Various methods of SHE is addressed in [11–14]. The four-quadrant functioning of SHE is explored in [15]. SHE method with a fewer DC source based MLIs are discussed in [16, 17]. The author in [18] implements a parallel resultant -based SHE strategy. In this technique, the proposed inverter has high number of switches. SHE technique with PV system and DC-DC converter fed MLI is discussed in [19]. But low gain DC-DC boost converter having high voltage stress are used for boost converter switch.

All the existing problems are overcome in the proposed work. In this proposed system, the input voltage from the photovoltaic system is fed into the High gain DC-DC SEPIC (Single Ended Primary Inductor converter) converter. The GWO algorithm-based PI controller fine tunes the output voltage. The different output voltages are given to the proposed reduced switch 31- level inverter.High frequency modulation method and SHE method is used for controlling the inverter.The comparison result shows the THD parameters in the result and discussion chapter.

3. Proposed System

The proposed PV fed high gain SEPIC Converter based reduced switch asymmetrical 31- level inverter is shown in figure 1.The extremely underdamped voltage from the photovoltaic system is fed into the SEPIC Converter, which provides a stable input current. Theessential DC output voltage to the MLI is achieved by using the Grey Wolf optimization algorithm.The reference voltage and actual voltages are compared and then the error is given to the comparator. Actual voltage is measured from

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output of the SEPIC Converter. The error is given to the PI controller. The PI controller minimizes error and generates a reference voltage signal for the generation of PWM. The GWO algorithm adjusts the gains of the PI controller. To generate a PWM pulse, the generated reference value is equated with the carrier value. The SEPIC Converter receives the triggering signals. The RSMLI receives four input voltages from the SEPIC Converter. The RSMLI in the proposed system is composed of a single H Bridge and a voltage multiplier circuit. The power circuit contains eight MOSFETs and 4 DC inputs. Multi Carrier Modulation is used to power the MLI. MCM is often referred to as high frequency modulation. The THD as well as the switching losses are severe in high frequency modulation schemes. To address these problems, a SHE algorithm based on Bee colony optimization is used. The degree of harmonics is compared to the genetic algorithm.

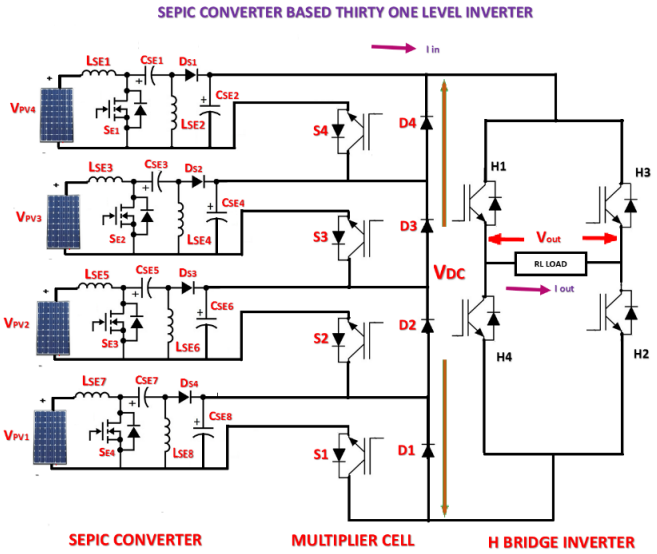

Figure 1. Proposed System Circuit diagram

4. GWO ALGORITHM

The SEPIC Converter output voltage V_{DC} and reference voltage V_{ref} are compared and the error is given to the PI controller. The error voltage can be calculated as,

$$\Delta Verr(n) = V\,ref(n) + V\,De(n) \quad (1)$$

The output of PI controller is presented as,

$$Iref = K\,p1\,(\Delta Verr(n) - \Delta Verr(n-1) + KI1\,.\Delta Verr(n) \quad (2)$$

The role of GWO algorithm is to calibrate the K_p and K_i values.

The grey wolf optimization technique is modelled after the grey wolves' traditional hunting behavior in nature, which is focused on their management hierarchy and traditional hunting mechanism. This method emulates the hierarchical system by using four different types of wolves, namely alpha (α), beta (β), gamma (δ), and omega (ω). Because the α wolf is regarded as the optimal solution, it is regarded as the team leader and commander of the hierarchy. The wolves' β andδ are regarded as 2nd and 3rd best

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solutions, respectively, assisting the wolf in solving problems. Finally, ω signifies the wolves which remain behind the leaders. The simulation outcomes describe the attack behavior in the algorithm.

$$\vec{e} = |\vec{f}.\vec{x}p(t) - \vec{x}p(t)| \quad (3)$$

$$\vec{x}(t+1) = \vec{x}p(t) - \vec{a}.\vec{e} \quad (4)$$

where t is the current iteration, a, e and f represent the coefficient vectors, xp specifies the position vector of the prey and x refers to the position vector of grey wolf. The vectors a and f are computed as follows:

$$\vec{a} = 2.\vec{b}.\vec{r1} - \vec{b} \quad (5)$$

$$\vec{f} = 2.\vec{r1} \quad (6)$$

Where the components of $b^{\rightarrow}$ decrease linearly from 2 to 0; $r1^{\rightarrow}$, $r2^{\rightarrow}$ are random vectors in [0, 1].

5. Selective Harmonic Elimination Technique

The output voltage of the inverter can be presented as ,

$$V\omega t = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \quad (7)$$

Where,

V_n – The nth harmonic switching angles are limited in amplitude to zero and 90^{θ} ($0 <= \theta_i <= \frac{\pi}{2}$).

The even harmonics are equated to zero

$$V\omega t = \frac{4}{n\pi}[V_1\cos(n\theta_1) + V_2\cos(n\theta_2) \ldots\ldots\ldots\ldots + V_n\cos(n\theta_n)]\sin n\omega t \quad (8)$$

Where n=1, 3, 5, 7

Shortly

$$Vn = \begin{cases} \frac{4}{n\pi}\sum_{i=1}^{S}\cos(n\theta_1) & for\ odd\ ns \\ 0 & for\ even\ ns \end{cases} \quad (9)$$

The proposed thirty-one level inverter can reduce the harmonics up to 15 th order. To remove these 15 orders of harmonics 15 trigonometric nonlinear equations are solved and 15 triggering angles are obtained. Equation 10 is solved for obtaining the triggering angles.

$V_1\frac{4}{\pi}[V_1\cos(\theta_1) + V_2\cos(\theta_2) \ldots\ldots\ldots\ldots + V_{15}\cos(\theta_{15})]$

$V_3\frac{4}{3\pi}[V_1\cos(3\theta_1) + V_2\cos(3\theta_2) \ldots\ldots\ldots\ldots + V_{15}\cos(3\theta_{15})]$

$V_5\frac{4}{5\pi}[V_1\cos(5\theta_1) + V_2\cos(5\theta_2) \ldots\ldots\ldots\ldots + V_{15}\cos(5\theta_{15})]$

.

.

$$V_{15}\frac{4}{15\pi}[V_1\cos(15\theta_1) + V_2\cos(15\theta_2) \ldots\ldots\ldots\ldots + V_{15}\cos(15\theta_{15})] \quad (10)$$

6.Results and Discussion

The proposed work has been implemented in Matlab simulation and hardware is implemented using

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DSPIC30F2010 controller. The solar panel output is given to the SEPIC converter, the converter output voltage is fed to multilevel inverter. The figures from 2 to 21 shows the simulation and hardware results of proposed system.The table 1 shows the parameters of solar panel used in this system.The figure 2 shows the output voltage from the PV panel.

Table 1. Solar panel rating details

COMPONENTS	SPECIFICATIONS
Number of panels	4
Number of cells in series	36
Cell	$125mm \times 31.25mm$
Open circuit voltage	$21.4V$
Optimum operating voltage	$16.8V$
Short circuit current	$1.21A$
Optimum operating current	$1.19A$
Operating temperature	$-40\ to\ +850C$
Maximum system voltage	$1000V\ DC$

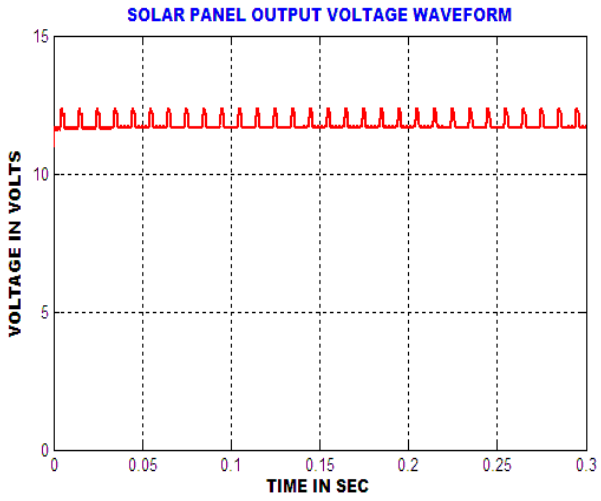

Figure2. Simulation Output of PV system

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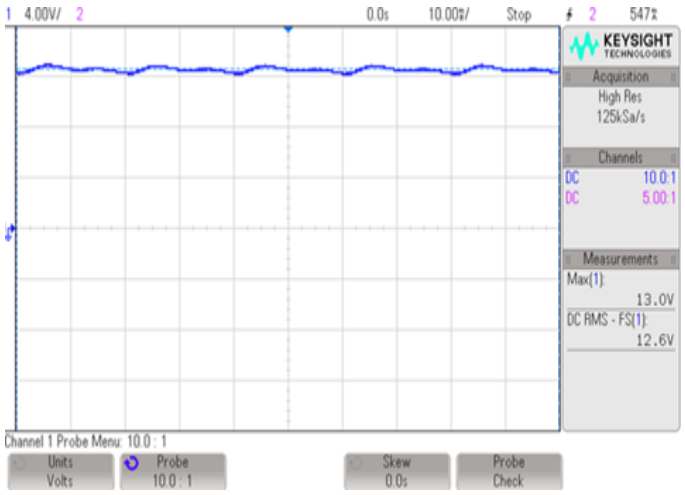

Figure3. Hardware Output of PV system

The four DC voltages are with range of 6, 12, 24 and 48 V. The figure 3 shows the output voltage of the SEPIC converter. Theratings of the SEPIC converters are given in following table 2.

Table 2. Parameters of SEPIC converter

Components	**Symbols**	**Rating**
Source Voltage	v_{in}	6 to 20 V DC.
Source Current	i_i	11 A
Capacitors	C_1,C_2	50uf/100v
Inductor	$L1, L2$	1Mh
Output load current		1 Amps
Switching frequency	f	10 KHZ
Output Power	P_0	200W
Switching devices(all)		IRF250
Diodes(all)		MUR1560
Driver Circuit		TLP 250

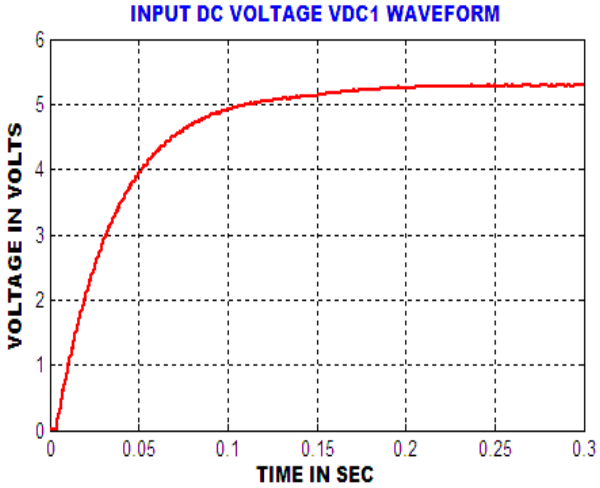

Figure4. Simulation output of VDC1

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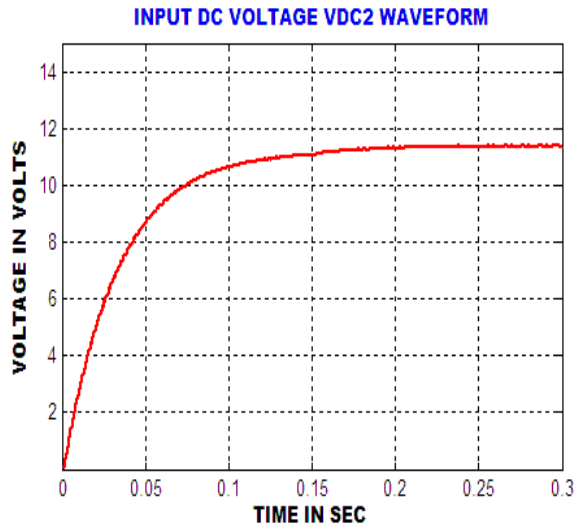

Figure5. Simulation output of VDC2

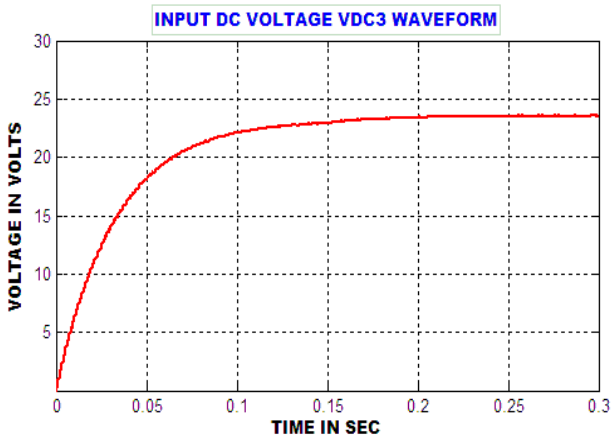

Figure6. Simulation output of VDC3

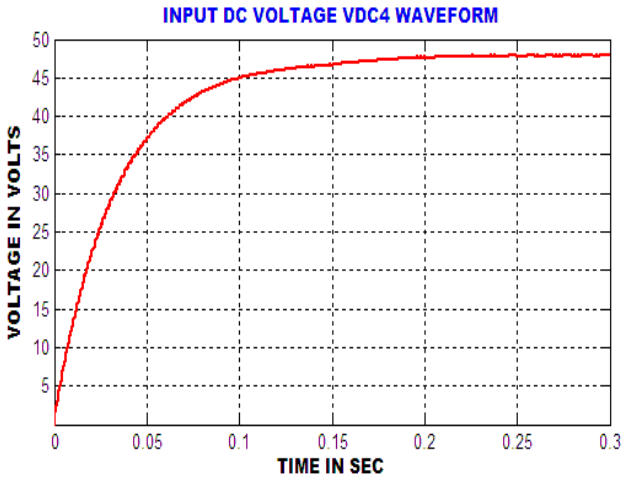

Figure7. Simulation output of VDC4

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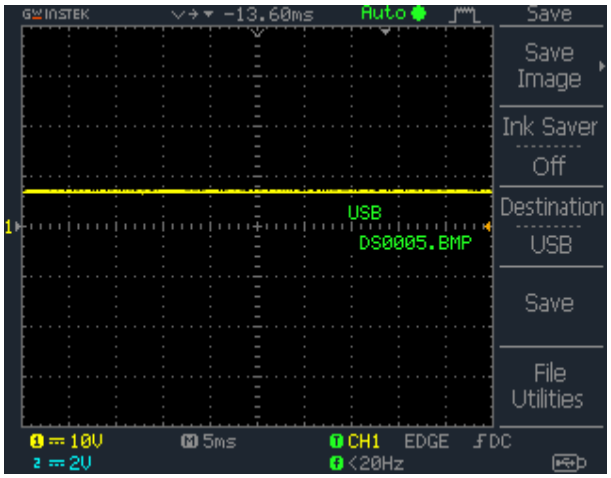

Figure8. Hardware output of VDC1

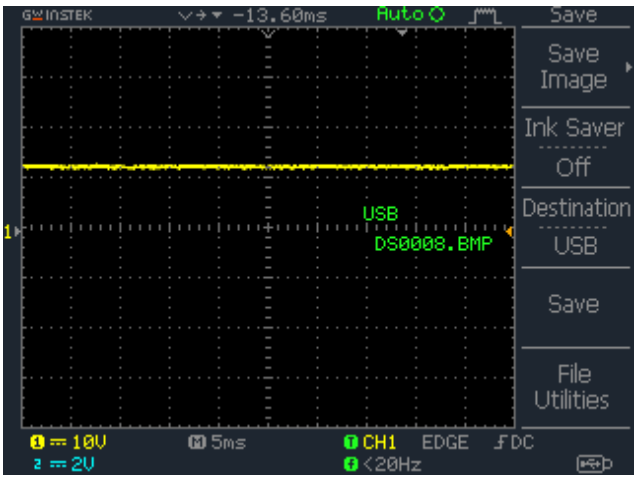

Figure9. Hardware output of VDC2

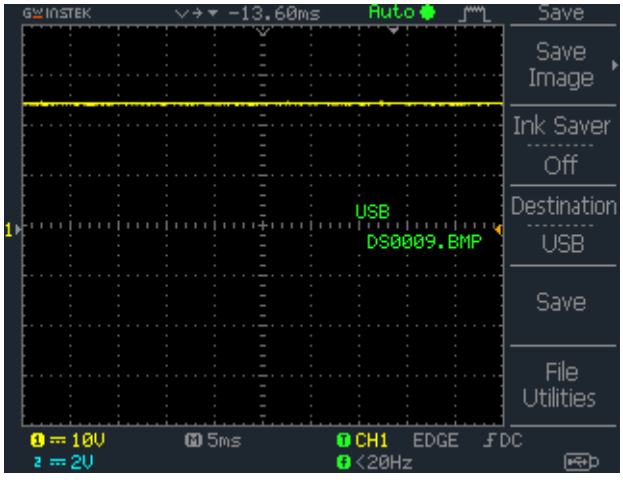

Figure 10. Hardware output of VDC3

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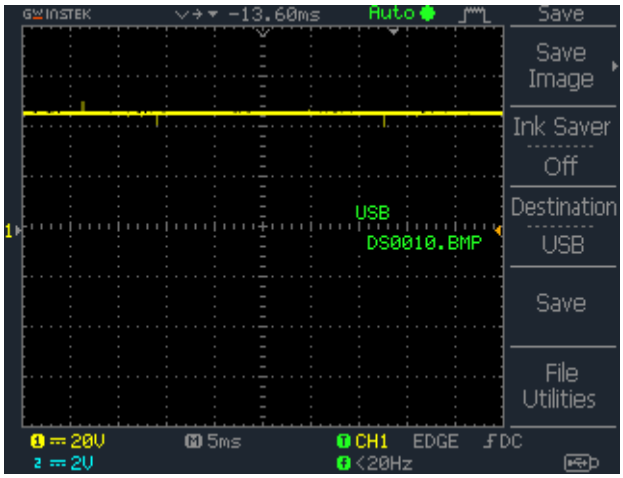

Figure 11. Hardware output of VDC4

The figure 12 shows the thirty-one-level inverter voltage waveform using MCM with MI= 0.95.The MCM technique is used to regulate the multilevel inverter. The reference signal is produced using PI controller. The output voltage of the thirty one level inverter is given below.

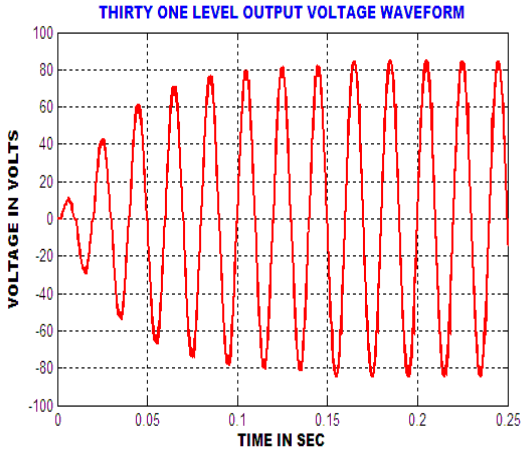

Figure 12. Simulation output of Thirty one level inverter (MCM)

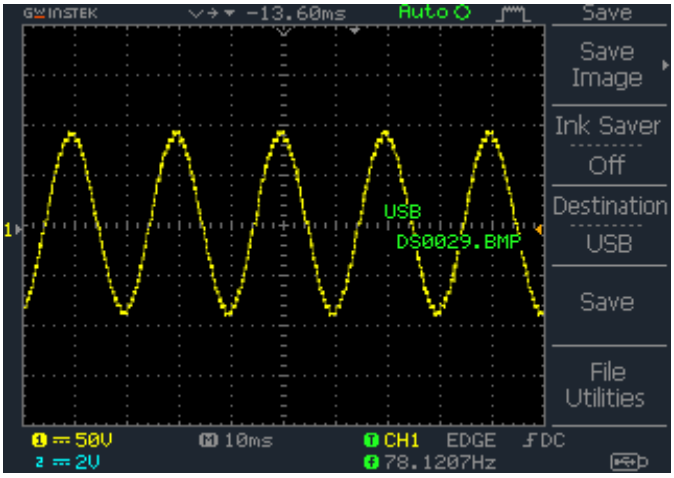

Figure 13. Hardware output of Thirty one level inverter (MCM)

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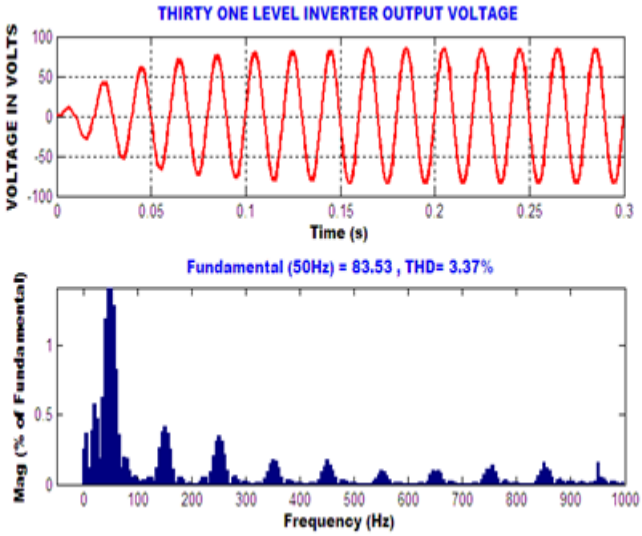

Figure 14.%THD of 31-level inverter using MCM method

Table3 presents the triggering angles calculated using BCO. The triggering pulsesto the proposed inverter is fed using DSPIC30F2010 controller.

Table 3. Switching angles using SHE-BCOmethod

ANGLE	$\alpha 1$	$\alpha 2$	$\alpha 3$	$\alpha 4$	$\alpha 5$	$\alpha 6$	$\alpha 7$	$\alpha 8$	$\alpha 9$	$\alpha 10$	$\alpha 11$	$\alpha 12$	$\alpha 13$	$\alpha 14$	$\alpha 15$
ABC-SHE	5.97	11.02	16.7	22.6	29.1	34.8	41.6	47.6	52.9	58.7	65.2	71.1	77.3	83.1	89.6
GA	5.98	10.97	16.9	23.1	29.3	35.2	40.7	46.8	53.2	57.6	64.3	70.2	77.1	82.8	88.9

The figure 15 presents the shows simulation and hardware results of SHE-BCO method.

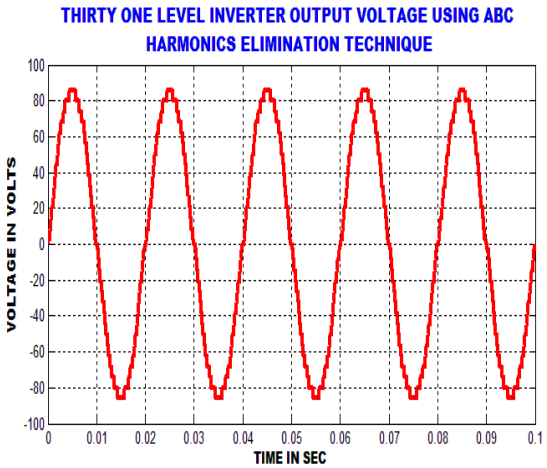

Figure15. Simulation output of SHE-BCO method

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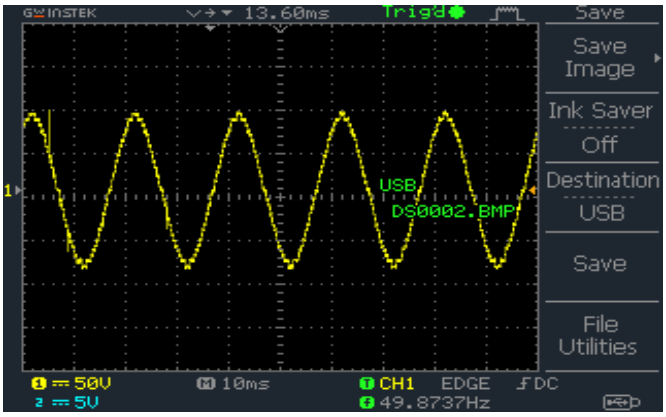

Figure16. Hardware output of SHE-BCO method

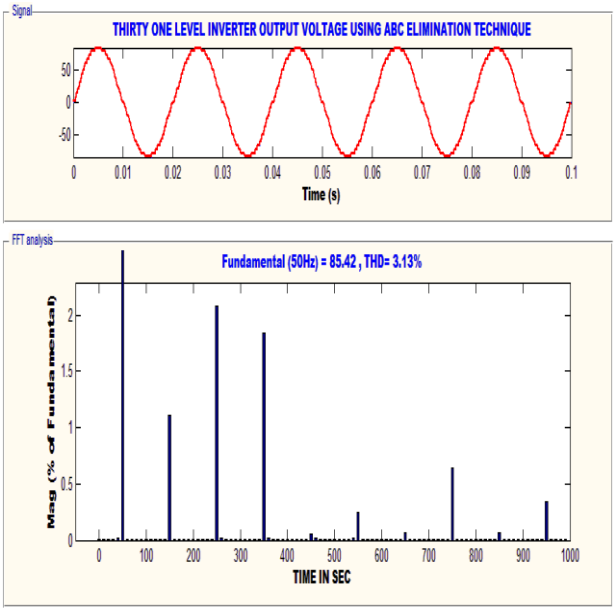

Figure17.%THD of 31-level inverter using BCO method

The figure 18 presents the shows simulation and hardware results of SHE-GA method

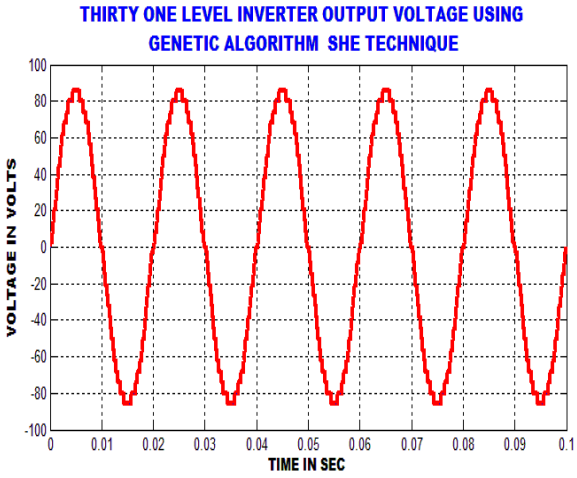

Figure18. Simulation output of SHE-GA method

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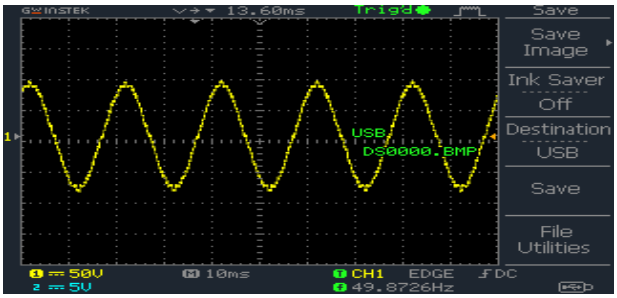

Figure19. Hardware output of SHE-GA method

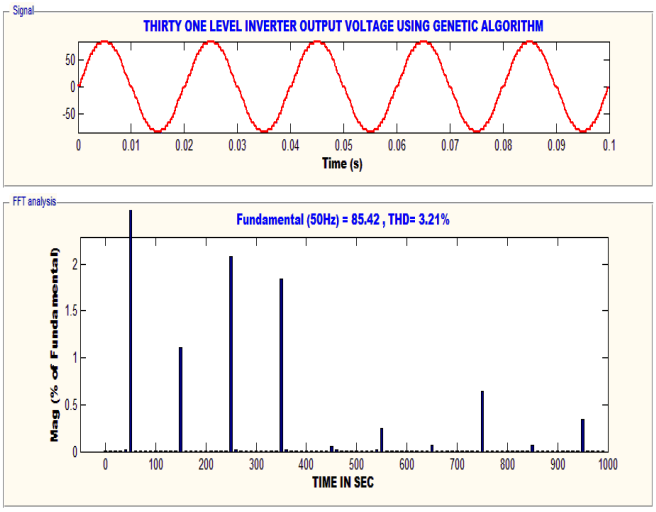

Figure 20.%THD of 31-level inverter using GA method

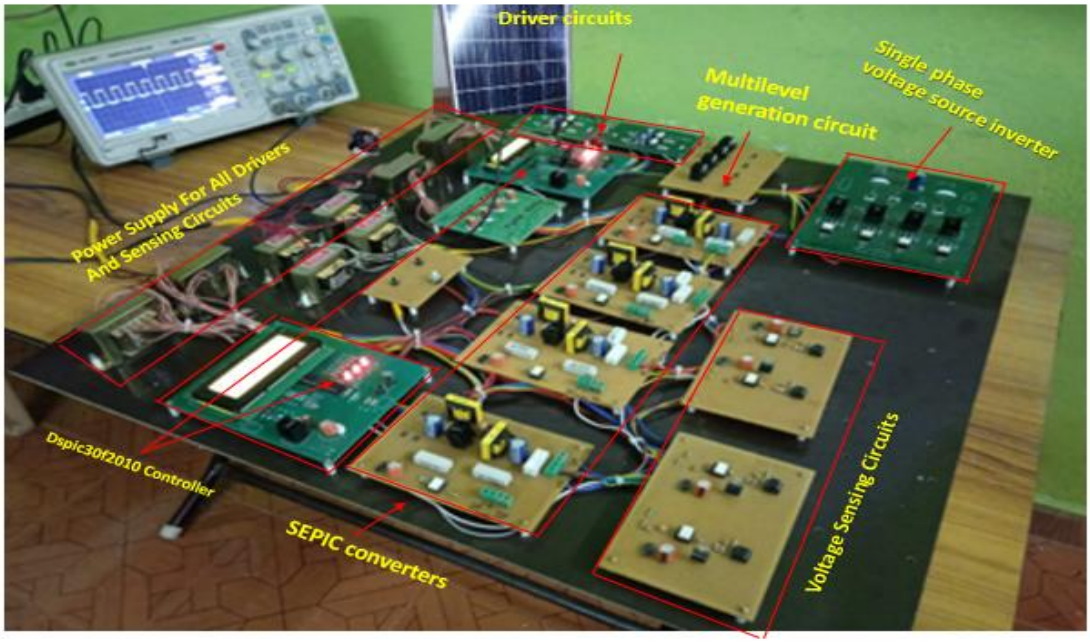

Figure 21. Experimental setup for proposed system

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CONCLUSIONS

In this paper, the BCO and GA-based SHE methods are used primarily to reduce lower order harmonics. The Grey Wolf Optimizer maximizes the performance of the photovoltaic system by tracking maximum power with the help of SEPIC converter. Moreover the proposed 31-level inverter was also analyzed using MCM method. Finally, the THD's of the two SHE strategies and the MCM methods are compared, and it is discovered that the BCO SHE method gives a lower harmonic content than the other two methods. The research approach has been validated using Matlab software, and the hardware tests have been validated using DSPIC30F2010 controller simulation.

References

[1] Ch.Rambabu et al. "A Novel 7-Level Parallel Current Source Inverter for High Power Application with DC Current Balance Control", International Journal of Electronics & Communication Technology, Vol-3, Issue–4, PP: 73-79, Oct – Dec 2012.

[2] Ch.Rambabu et al. "A New Topology for Cascaded Multilevel Inverters with Single DC Input" International Journal of Advances in Engineering Research, Vol. No. 2, Issue No. II, August 2011.

[3] 13. Ch. Rambabu et al. "A Novel Multi Level Inverter Topology By Using Switched Capacitor Connection", International journal of professional Engineering studies, Vol.2, No.2, March 2014, pp.41-46.

[4] Mahrous Ahmed, Mohamed Orabi, Sherif Ghoneim, Mosleh Alharthi, Farhan Salem, Bassem Alamri & Saad Mekhilef (2019) Selective harmonic elimination method for unequal DC sources of multilevel inverters, Automatika, 60:4, 378-384, DOI: 10.1080/00051144.2019.1621048

[5]Javier Chavarria; Domingo Biel; FrancescGuinjoan; Carlos Meza and Juan J. Negroni, Year: 2013 , "Energy-Balance Control of PV Cascaded Multilevel Grid-Connected inverters Under Level-Shifted and Phase-Shifted PWMs", IEEE Transactions on Industrial Electronics, vol. 60 , no. 1,pp. 98 – 111.

[6] Sze Sing Lee, Year: 2018 , "A Single-Phase Single-Source 7-Level Inverter With Triple Voltage Boosting Gain", IEEE Journals & Magazines, vol. 6, pp. 30005 – 30011.

[7]G. Irusapparajan, D. Periyaazhagar, N. Prabaharan & A. Rini ann Jerin (2019) Experimental verification of trinary DC source cascaded H-bridge multilevel inverter using unipolar pulse width modulation, Automatika, 60:1, 19-27, DOI: 10.1080/00051144.2019.1570643

[8] Gerardo Escobar Valderrama; Gerardo Vazquez Guzman; Erick I. Pool-Mazún;Panfilo Raymundo Martinez-Rodriguez ; Manuel J. Lopez-Sanchez and Jose Miguel Sosa Zuñiga, Year: 2018 , "A Single-Phase Asymmetrical T-Type Five-Level Transformerless PV Inverter", IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6 , no. 1, pp. 140 – 150.

[9]Ruoshui Ni; Yun Wei Li; Ye Zhang; Navid R. Zargari and Zhongyaun Cheng, Year: 2014, "Virtual Impedance-Based Selective Harmonic Compensation (VI-SHC) PW for Current Source Rectifiers", IEEE Transactions on Power Electronics, vol. 29 , no. 7,pp. 3346 – 3356.

[10Evren Isen, Ahmet Faruk Bakan. (2016) Development of 10 kW Three-Phase Grid Connected Inverter. *Automatika* 57:2, pages 319-328.

[11]AyoubKavousi;BehroozVahidi; Reza Salehi; Mohammad KazemBakhshizadeh; NaeemFarokhnia and S. Hamid Fathi, Year: 2012 "Application of the Bee Algorithm for Selective Harmonic

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 10471 - 10484
Received 25 April 2021; Accepted 08 May 2021.

Elimination Strategy in Multilevel Inverters, IEEE Transactions on Power Electronics, vol. 27 , no. 4, pp. 1689 – 1696.

[12]Shunmugham Vanaja, D., Albert, J.R. and Stonier, A.A., 2021. An Experimental Investigation on solar PV fed modular STATCOM in WECS using Intelligent controller. International Transactions on Electrical Energy Systems, p.e12845.

[13]Shunmugham Vanaja, D. and Stonier, A.A., 2020. A novel PV fed asymmetric multilevel inverter with reduced THD for a grid-connected system. International Transactions on Electrical Energy Systems, 30(4), p.e12267.

[14]Shunmugham Vanaja, D. and Stonier, A.A., 2021. Grid integration of modular multilevel inverter with improved performance parameters. International Transactions on Electrical Energy Systems, 31(1), p.e12667.

[15]Hui Zhao and Shuo Wang, March 2017,"A Four-Quadrant Modulation Technique to Extend Modulation Index Range for Multilevel Selective Harmonic Elimination Compensation using Staircase Waveforms",IEEE Journal of Emerging and Selected Topics in Power Electronics , vol. 5 , no. 1, pp. 233 – 243.

[16] KazemHaghdar and Heidar Ali Shayanfar, Year: 2018, "Selective Harmonic Elimination With Optimal DC Sources in Multilevel Inverters Using Generalized Pattern Search",IEEE Transactions on Industrial Informatics, vol. 14, no. 7, pp. 3124 – 3131.

[17] ConcettinaBuccella; Carlo Cecati; Maria Gabriella Cimoroni and KavehRazi, Year: 2014, "Analytical Method for Pattern Generation in Five-Level Cascaded H-BridgeInverter Using Selective Harmonic Elimination", IEEE Transactions on Industrial Electronics, vol. 61 , no. 11, pp. 5811 – 5819.

[18] Muhammad Bilal Waheed, Abdul Rauf Bhatti, Muhammad Amjad, Yasir Saleem, Shahab Ahmad Niazi, Suhail Khokhar. (2019) A Simplified Model Predictive Control of Four-Leg Two-Level Inverter. *Electric Power Components and Systems* 47:14-15, pages 1287-1302.

[19] FaeteFilho; Leon M. Tolbert; Yue Cao and BurakOzpineci, Year: 2011, "Real-Time Selective Harmonic Minimization for Multilevel Inverters Connected to Solar Panels Using Artificial Neural Network Angle Generation", IEEE Transactions on Industry Applications, vol. 47 , no. 5, pp. 2117 – 2124.