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Cost effective universal shift register in quantum dot cellular automata using clock zone-based crossover

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Abstract: Quantum-Dot Cellular Automata (QCA) is a modern nanotechnology, which uses quantum cells to express the binary information without current flow. It has emerged as suitable alternative to current CMOS architecture. The design of combinational and sequential circuit seems to be a challenging task in QCA technology. In this paper, a novel cost effective universal shift register is proposed. Initially a novel 2 to 1 multiplexer and D flip-flop with fewer numbers of majority gate and inverters are designed. Then these proposed designs are utilized to build the cost effective universal shift register. Here the clock zone-based crossover (CZBC) is used for interconnection to reduce the circuit complexity and cost function of the proposed design. Using the QCA designer environment and QCAPro designer tool, the proposed design is experimentally verified and tested for overall energy dissipation. As compared to the existing literature, the simulation result shows that the proposed configuration reduces cell count by 38%, majority gate by 30% and latency by 68%. The proposed clock zone-based crossover universal shift register (CZBCUSR) achieves 23% better QCA cost function and 32% higher device density due to utilization of CZBC, lesser number of majority gate and inverter.

Keywords: Universal Shift Register, Multiplexer, D flip-flop, Coplanar Crossover, Multilayer Crossover, Clock Zone Based Crossover (CZBC), QCA Cost Function.

1. INTRODUCTION

Realization of digital circuits has detected deliberate challenges caused due to the scaling down of CMOS technology, by means of short channel effects, impurity variation, and huge leakage power dissipation [1]. Due to these challenges, Lent et.al introduced the quantum dot cellular automata in 1993 [2], as an attractive alternative for CMOS design [3]. From the last decade, QCA has received much more attention because of its attractive features like, power consumption, Terahertz frequency of high-speed operation [4] and high device density [5]. Apart from all the benefits, QCA continues to suffer from room temperature during fabrication, as QCA cells operate only in cryogenic temperature. Recently, Diabio et.al successfully fabricated the electrostatic QCA cell, which is able to function in and above 293 Kelvin [6]. This breakthrough invention gives big inspiration to the researchers for further implementation of QCA based circuits. More number of logical architectures has been implemented in both combinational and sequential circuits, since the inception of QCA technology.

The universal shift register (USR) is a digital circuit that is widely used in memory units, data storage, and data manipulation. This kind of USR is constructed by using the multiplexer and shift register [7]. In USR, a multiplexer is needed to perform a single operation at a time, and shift register is used to perform right shift and left shift [8, 9].

In literature, only limited QCA based USRs are reported [10-13] from the reported works it may be found that QCA based USR circuits realized using flip-flop and multiplexer have been extensively studied [14-17] due to their wide range of application in digital systems. In [10], multiplexer is realized by using a majority gate and a robust inverter, with a signal distribution network (SDN), which is used to overcome the crossover issue. Hence, it increases the area and cell count of the USR circuit. In [11], reset ability flip-flop is used to design a shift register, which is realized by using the majority gate and a robust inverter. Latency of the circuit is reduced by 50% in [11], when compared to the previous literature, but an excessive consumption of greater number of QCA cells and occupancy of more area is occurred. Moreover, it employs a multilayer crossover function, which increases the fabrication difficulty and cost function of the QCA circuit. In [12], QCA USR is realized by the multiplexer and D flip-flop. Unlike the earlier designs, the multiplexer is constructed by realizing electronic correlation between the cells. D flip-flop is constructed by a simple inverter and two AND gates, with common reference nodes, which reduces the device density. In addition, it requires coplanar or multilayer wire crossings. In [13], two-bit USR is designed with fault tolerant features. To avoid cell misplacement errors, rotated majority gates (RMGs) are used to construct, D flip-flop and multiplexer. RMG is constructed by using 45º rotated QCA wires (i.e) coplanar crossover which increases the fabrication complexity of the circuit.

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In literature [11-12], USR is constructed by multilayer crossover and in [13], it is constructed by coplanar crossover. Earlier research has demonstrated that multilayer QCA circuits exceed coplanar circuits in terms of latency, area and number of QCA cells [18, 19]. However, the multilayer QCA crossovers circuits attained the advantage in terms of area, which increases the fabrication cost of the circuit [20]. Both types of crossovers have their own disadvantages. To overcome these disadvantages, the novel clock zone-based crossover (CZBC) universal shift register (USR) is efficiently proposed with reset ability; it is achieved by the use of novel 4 to 1 multiplexer and D flip-flop. Multiplexer is designed by considering logical inherent characteristics of quantum-dot cellular automata technology, which reduces the cell count. D flip-flop is designed with novel architecture to increase the efficiency of the circuit with reduced latency. Shift register is build by using a proposed multiplexer and D-flip flop. The hindrances of coplanar and multilayer crossover issues are eluded in proposed design, by employing CZBC technique, in order to accomplish high device density, with much less fabrication complexity. The proposed structures, namely, the multiplexer, D flip-flop and shift register have its own energy dissipation, which is determined by the QCAPro designer tool [21].

In this paper, QCA's history is explained in section 2; section 3 addressed the proposed multiplexer and D – flip flop, which is also used to construct a 4-bit clock zone-based crossover universal shift register layout. Novel layout of 4-bit clock zone-based crossover universal shift register implementation is modeled and the simulation results were addressed in Section 4. Evaluation of proposed D flip-flop and multiplexer configurations on energy dissipation is depicted in section 5. The QCA cost function of the novel CZBCUSR is described in section 6. In section 7 the performance of the proposed design is compared with the existing literature. The results in section 6, shows that the proposed design improves its efficiency towards area and QCA cost function than the other QCA based USR in the literature.

2. PRELIMINARIES OF QUANTUM-DOT CELLULAR AUTOMATA

A. Quantum Dots, QCA Cell and Tunnel Junctions

A quantum dot is a piece of space in a QCA cell, surrounded by a tunnel junction that is extensive enough to quantify the charge within multiple elementary charges. At some stage, the barriers must be sufficiently apparent to allow a charge that may mechanically tunnel to another dot [22]. The group of four "dots'' sited in the boundaries of the square together frames a QCA cell. The cells accommodate two additional migrant electrons that can tunnel mechanically among the dots, not between the cells. Due to Coulomb interaction, the electrons repulse each other and they tend to achieve maximum separation by holding the dots in the antipodal direction. Based on columbic interaction between the mobile electrons, the antipodal sites can be occupied by them through tunneling junctions as depicted in Fig. 1.

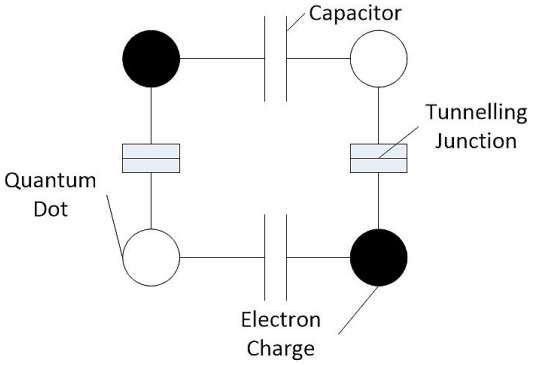

Figure 1. QCA Cell configuration

Moreover, depending on the arrangement of electrons, two cell orientations are possible. Those possible orientations are utilized for the representation of the binary '0' and binary '1' [6] as illustrated in Fig. 2. The corresponding polarization measurement is calculated by (1). The indexing of dots in the cell (referred as CP_i) begins in clockwise direction from the top right that follows bottom right, bottom left and top left which is numbered as 1,2,3,4.

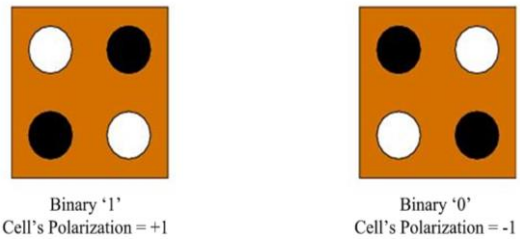

Figure 2. QCA Cells with its polarization

$$\text{Cell's Polarization (CP)} = \frac{(CP_1+CP_3)-(CP_2+CP_4)}{(CP_1+CP_2+CP_3+CP_4)} \qquad (1)$$

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Array of QCA cells forms QCA wires. Depending on the alignment of dots in QCA cells, it is classified into two structures, namely; normal wire and rotated wire. In normal wire, dots in QCA cell consist of 90º alignment and rotated wire consist of 45º alignment [23]. Based on the alignment the structure of wires are presented in Fig. 3

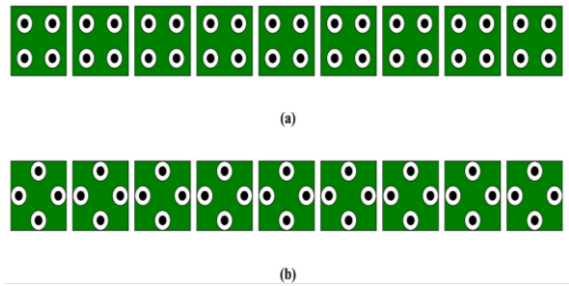

Figure 3. Wires in QCA (a) 90º (Normal Wire) (b) 45º (Rotated Wire)

B. Logic primitives in QCA

Simple logic elements, namely, a majority gate and an inverter, can be constructed in QCA, on the basis of cell-to-cell interactions. If two typical 90º QCA cells are diagonally positioned, they obtain opposite polarization and the device acts as inverter gate [24] due to electrostatic repulsion; this conversion of binary '0' and binary '1' takes place and vice versa. A robust and simple inverter is depicted in Fig. 4a and 4b. A majority gate is configured with the help of five QCA cells which carry out the operation based on (2).

$$Maj\ (A, B, C) = A.B + B.C + C.A \quad (2)$$

By using a fixed value for one of the inputs, AND or OR gate can be easily configured by using majority gates as shown in Fig. 4c and 4d. For example, out of three inputs in the majority gate, one of the inputs is fixed as '0' to build a two input AND, as in (3), likewise one of the inputs is fixed as '1' to build a OR gate as in (4).

$$AND\ (A, B, 0) = OUT\ (A \,\&\, B) \quad (3)$$

$$OR\ (A, B, 1) = OUT\ (A \mid B) \quad (4)$$

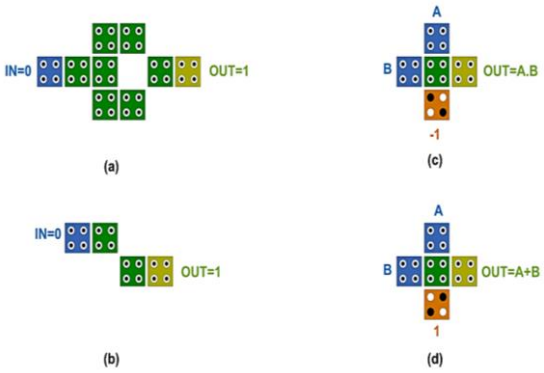

Figure 4. Representation (a) Robust Inverter (b) Simple Inverter (c) Majority AND gate (d) Majority OR gate

C. Wire crossing in QCA Logic circuits

One of the sole features of QCA's ability is to make diverse crossovers in QCA wire. In general, crossovers of wires in QCA circuits can be carried out by three different methods by QCA cell itself, namely coplanar crossover, multilayer crossover and clock zone-based crossover (CZBC). For the coplanar method, two orientations are needed in wires, one in 90º standard cells orientation and the other with 45º rotated cells orientation [25] as shown in Fig. 5a. It leads to low robustness and higher fabrication complexity. In addition, the design of coplanar crossover involves rotation of QCA cells, which significantly reduce the energy divergence among the QCA cells. High operating temperature and gradual reduction in the switching time are the outcomes, which in turn reduces its performance [26]. On the other hand, three or five layers is utilized in the multilayer crossover [27], and it is identical to metal wire routing technology, which is available in CMOS, as depicted in Fig. 5b. However, this type of crossover enhances the design efficiency with regard to area and latency; the fabrication complexity of this crossover will be higher than the coplanar crossover, which in turn increases the cost function of the QCA circuit. The clock zone-based crossover (CZBC) [28 - 30] fixes the above issues

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by employing only regular cells where the alternate clock zones between the wires are used as shown in the Fig. 5c [31]. Hence, this is the simplest approach to reduce the design complexity and fabrication issue [32].

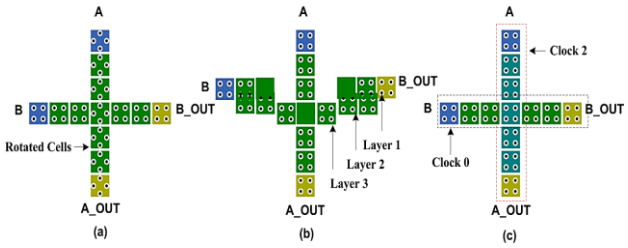

Figure 5. Crossover structure of (a) Coplanar (b) Multilayer (c) Clock Zone Based

D. Clocking in QCA

In QCA Circuits, synchronization and timings are done by QCA Clocking, and this type of clocking is achieved by two ways of switching; one is abrupt and the other is adiabatic [33]. The circuit goes to an excited state when the input of the QCA circuit is in abrupt switching. Whereas, in adiabatic switching, the dissipation of the energy to the environment is done by the QCA circuit in order to reach its ground state [34]. Therefore, the adiabatic switching takes precedence and the system is held in its instantaneous ground state at all time. In QCA, four distinct clocking phases are described accordingly as shown in Fig. 6. They are switch, hold, release and relax phases [33]. The polarization states of the electrons in the cells aids typically to acquire clocking. QCA clocking not only regulates the flow of information, but also serves as a power supply [35].

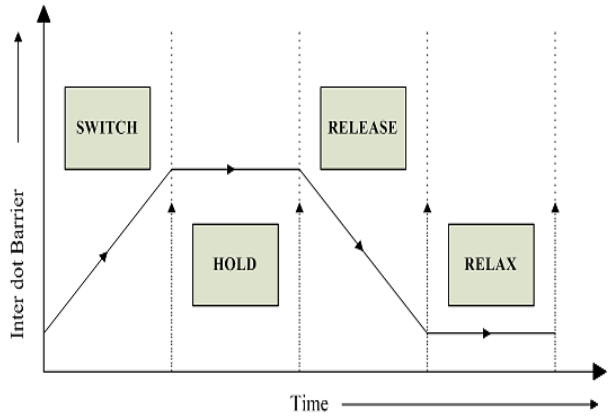

Figure 6. Clocking phases in QCA technology

3. PROPOSED LOGIC CIRCUIT IMPLEMENTATION

A. 2 to 1 Multiplexer

Multiplexer is a combinational circuit, which uses the select lines to get the output from any one of the input lines. From Table 1, it is clear that the I0 appears at the output line when SL = 0, and I1 appears, when SL = 1 [36]. Generally, the QCA based multiplexer structures are realized by using a “majority gate” and “inverter” logic elements. But the proposed structure shown in Fig. 7 does not require those logic elements. Instead, it takes the benefits of Quantum dot logical inherent characteristics to obtain the preferred output. The proposed structure consumes 12 numbers of QCA cells with 0.01 µm2 area and the corresponding output is depicted in Fig. 8. Three 2 to 1 multiplexers are utilized to design an optimal 4 to 1 multiplexer as shown in Fig. 9, in which, S0 is acted as a select line for first two 2 to 1 multiplexers and the third 2 to 1 multiplexer uses S1 as a select line; optimal design consumes 58 QCA cells and it occupies of 0.05 μm^2 area, which is approximately 20% lesser than [12]. In 4 to 1 multiplexer the select line values are 00, 01, 10 and 11 and the output s are I0, I1, I2 and I3 [37].

TABLE I. MULTIPLEXER TRUTH TABLE

2 Input Multiplexer		4 Input Multiplexer		
S	Out	S_0	S_1	Out
0	I_0	0	0	I_0

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1	I_1	0	1	I_1
		1	0	I_2
		1	1	I_3

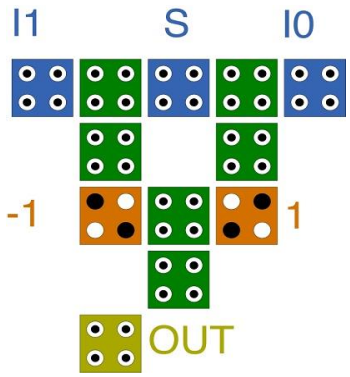

Figure 7. Novel 2 to 1 QCA Multiplexer Layout

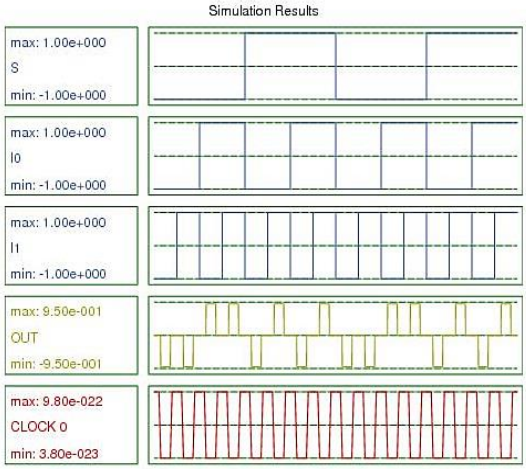

Figure 8. Output of Novel 2 to 1 QCA Multiplexer

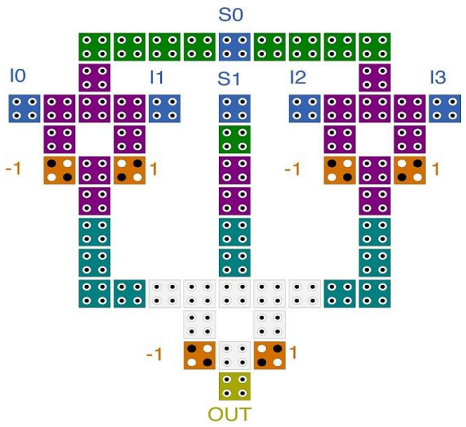

Figure 9. Novel 4 to 1 QCA Multiplexer Layout

B. D-flip-flop with clear input

The novel D flip-flop is constructed with CLR' input which is used to reset the flip-flop asynchronously. The logical D flip-flop represents the characteristic equation of Q = [((D.CLK) + (Q.CLK')). CLR'] and the related truth table is displayed in Table 2. In the proposed design, a simple inverter is utilized to build the D flip-flop, instead of a robust inverter, which is used in [11]. The area and cell count is diminished by the process of the first AND gate output cell being used as input cell for the OR gate. In the novel design, CLR' input is used to reset the register prior to its clock

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operation, which drastically reduces the latency of the circuit. The proposed D flip-flop consumed 17 numbers of QCA cells with 0.02 μm^2 area is depicted in Fig. 10 and the simulation result is illustrated in Fig. 11. Latency is reduced up to 25% than the existing D-FF in [12].

TABLE II. D FLIP-FLOP TRUTH TABLE WITH CLEAR INPUT

IN			OUT
CLR’	CLK	D	Q
0	X	X	0
1	0	0	$Q_{(t-1)}$
1	0	1	$Q_{(t-1)}$
1	1	0	0
1	1	1	1

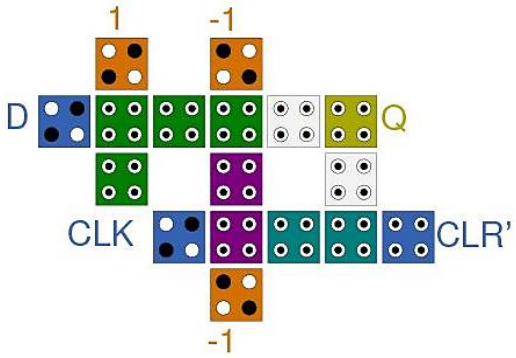

Figure 10. Proposed QCA D flip-flop layout with CLR’ input

C. Shift-Register

The binary information is stored in this logic design for short-term and it moves the stored information in a preset direction by one bit in each phase of clock [12]. In accordance with the input and output, shift registers are grouped into several forms. An optimal serial-in-parallel-out (SIPO) ‘shift-register’ using CZBC technique is designed in this paper.

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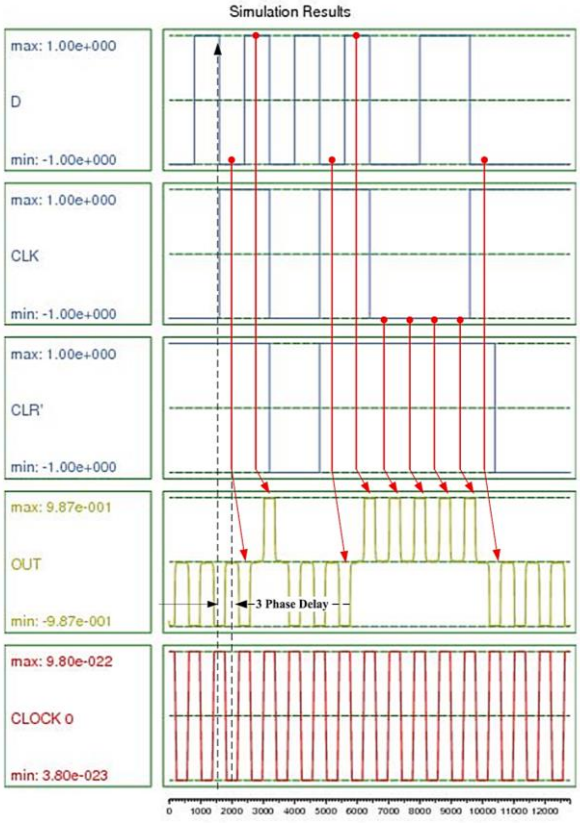

Figure 11. Output of proposed QCA D flip-flop layout with CLR' input

Foremost block in the SIPO consists of 'n' number of D flip-flops with common clock pulse, which simultaneously read or move output values to the next flip-flop in every clock pulse. The output of every single flip-flop is bridged to the input of the succeeding flip-flop in SIPO shiftregister [10]. A bit of information is loaded in the first clock pulse, and the formerly loaded information in the shift register is transferred to the next clock pulse towards the direction of either right or left. At the same time, the first flip-flop receives a new bit of information. In this paper, the SIPO shift register is realized by employing the novel D flip-flop owing to its ease implementation. The reset feature in the shift register is incorporated by utilizing the flip-flop with CLR' input. When the CLR' input is enabled, all the outputs become binary '0' at the same time as shown in Fig. 12. So many approaches are suggested to include reset ability into the flip-flop, such as connecting specific gates or multiplexers on the path of flip-flop's input or output [38, 39]. The best approach is to apply the reset input in the feedback loop in order to reduce the error probability which occurred after resetting [40]. The proposed reset ability SIPO shift register consumes a cell count of 132 cells with 0.11 µm2 area as shown in Fig. 12. Since it employs CZBC, fabrication complexity is drastically reduced. The proposed design needed 4 clock phase delay at each bit which is depicted in Fig. 13.

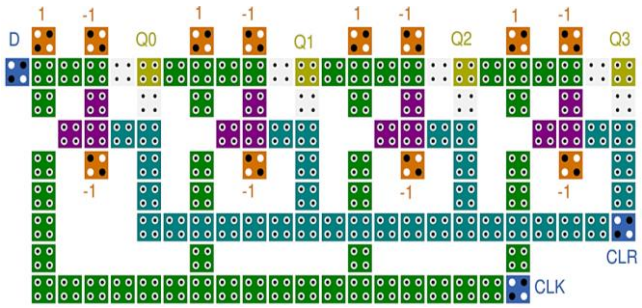

Figure 12. QCA layout of Serial-in – Parallel-out Shift register with proposed D flip-flop configuration

4. PROPOSED 4-BIT CLOCK ZONE-BASED CROSSOVER UNIVERSAL SHIFT REGISTER

The binary information in the universal shift register can be loaded, retrieved in either forms (serial or parallel) by moving it towards the right or left. A 4-bit USR exhibits four different operations which are depicted in Table 3. The logical model of 4-bit USR is depicted in Fig. 14. The proposed 4-bit clock zone-based crossover USR is depicted in Fig.

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15 and it uses four 4 to 1 multiplexers to drive the input pin of D flip-flop which is attached to the clock and CLR' input. Working algorithm of the proposed CZBCUSR is explained below.

Procedure CZBCUSR

Input I0, I1, I2, I3, CLK, CLR', S0, S1, SIRS, SILS;

Output Q0, Q1, Q2, Q3;

Begin

1. Declaring a condition for CLK to perform the CZBCUSR.
2. CLK is either '0' or '1'.
3. When CLK = 0; CZBCUSR remains same state.
4. When CLK = 1; CZBCUSR works on the following condition.

Begin

1. Declaring a condition for CLR' to perform the CZBCUSR.
2. CLR' is either '0' or '1'.
3. When CLR' = 0; CZBCUSR keeps data bit '0' in output.
4. When CLR' = 1; CZBCUSR works based on case condition.

Case 0: Remains Same

Case 1: Shift towards right side (SIRS)

Case 2: Shift towards left side (SILS)

Case 3: Parallel Load

end

end

endprocedure

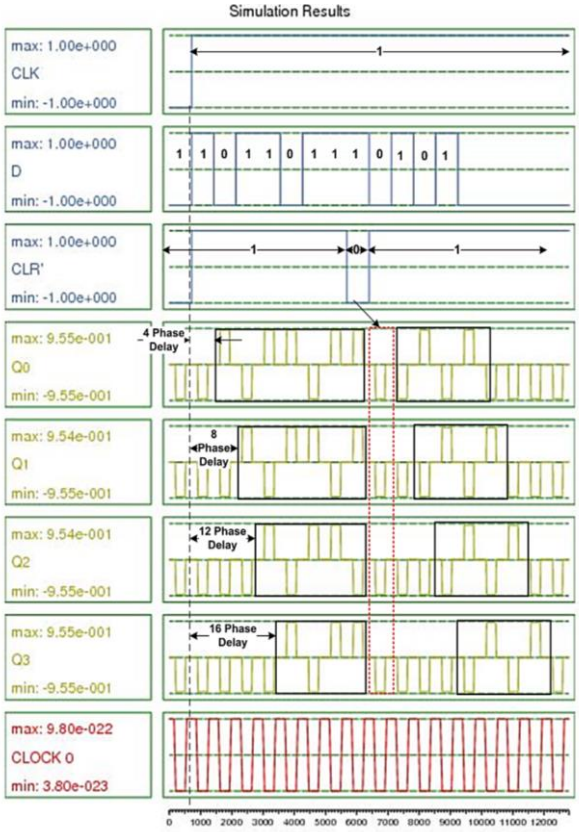

Figure 13. Output of Serial-in – Parallel-out Shift register

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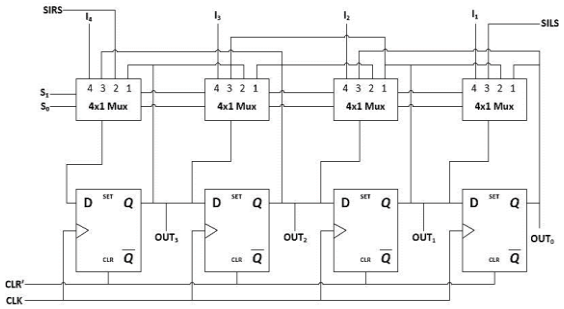

Figure 14. Logical Model for 4-bit Universal Shift Register

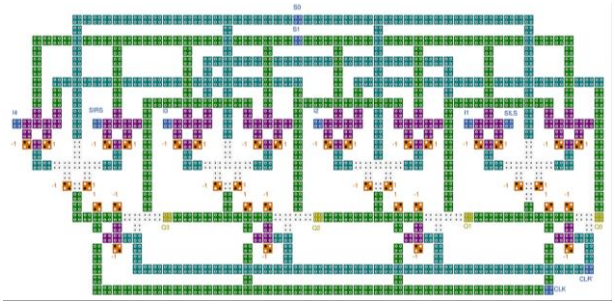

Figure 15. Proposed 4-bit Clock Zone-Based Crossover Universal Shift Register (CZBCUSR)

Select lines S_0 and S_1 are utilized to choose any one of the applications in the shift register, and these select lines are shared by all the four multiplexers presented in the 4-bit USR. When S_0S_1 = '00', no shift will occur for any number of clock cycles as the flip-flop's output is fed back to itself, and the corresponding simulation is shown in Fig. 16. While S_0S_1 = '01', data bits present in the register shifts to right side for each clock cycle with serial inputs '10110101' is being provided at second input Serial -In Right Shift (SIRS) of the left most 4 to 1 multiplexer, and the output is obtained at Out 0 (Q0), Out 1 (Q1), Out 2 (Q2) and Out 3 (Q3) respectively as shown in Fig. 17. Similarly, S_0S_1 = '10', data bits present in the register shifts to left side for each clock cycle with serial inputs '10110101'; it is being provided at third input Serial -In Left Shift (SILS) of the right most 4 to 1 multiplexer, and the simulated output is obtained at Q0, Q1, Q2 and Q3 respectively as shown in Fig. 18. During S_0S_1 = '11' the data inputs I1, I2, I3 and I4 appear at the register's output at the same time as shown in Fig. 16. CZBC technique is employed to design a USR to boost the switching time and to lessen the manufacturing complexity. The proposed CZBCUSR with reset ability consumes 705 cells with 0.70 μm^2 area.

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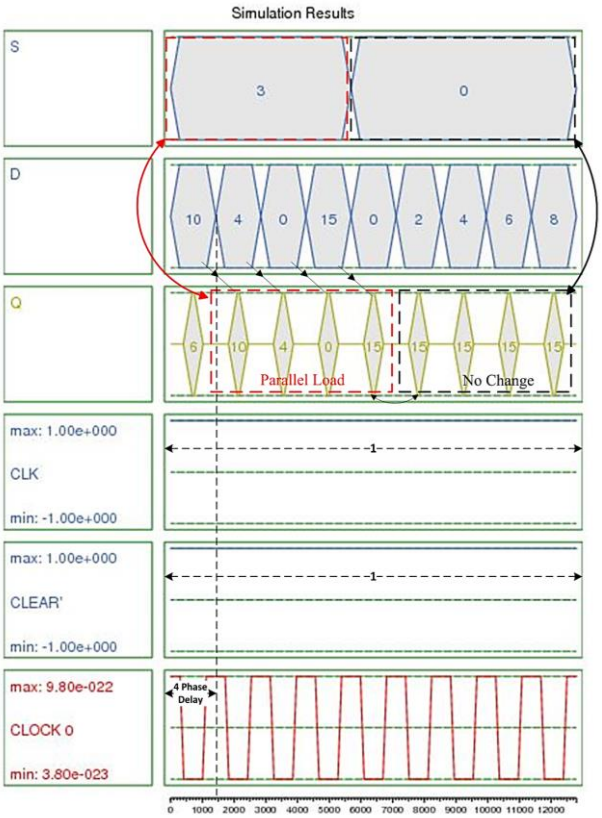

Figure 16. Simulated output of 4-bit CZBCUSR with S_0S_1='11' & '00'

TABLE III. FOUR BIT USR OPERATION

Select Lines of 4 to 1 Multiplexer		**Operations**
S_1	**S_0**	
0	0	Remains Same
0	1	Shift towards right side (SIRS)
1	0	Shift towards left side (SILS)
1	1	Parallel Load

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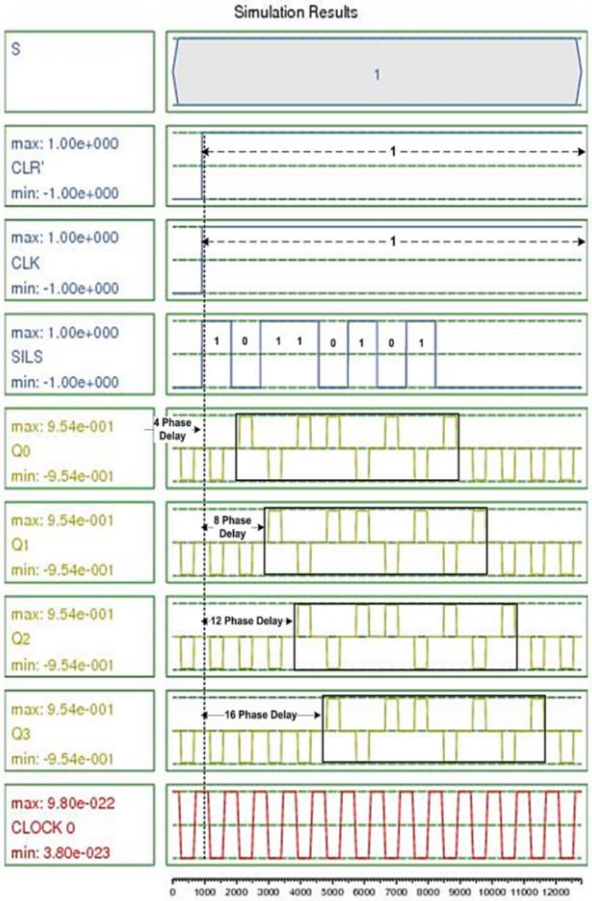

Figure 17. Simulated output of 4-bit CZBCUSR with S_0S_1='01' (SIRS)

5. ANALYSIS OF QCA ENERGY DISSIPATION

To estimate the design efficacy of a digital circuit, energy dissipation is considered as an important factor. For QCA circuit, the first power calculation formalism is established by Timler and Lent [41]. In their formalism, the total energy of a QCA cell is calculated by Hamiltonian matrix. Whereas, Hartree-Fock approximation is used for array of QCA cells by examining the columbic relationship of the cells by a mean field method [41, 43], which is exposed as,

$$\overline{H}=\begin{pmatrix} -\frac{E_k}{2}\sum_{i\neq j} d_{i,j}\, p_n & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_{i\neq j} d_{i,j}\, p_n \end{pmatrix}=\begin{pmatrix} -\frac{E_k}{2}\left(p_{j-1}+p_{j+1}\right) & -\gamma \\ -\gamma & \frac{E_k}{2}\left(p_{j-1}+p_{j+1}\right) \end{pmatrix} \quad (5)$$

In the above equation, the polarization of n^{th} adjacent cell is denoted as P_n and the electrostatic communication of the two logic states of the cells 'i' and 'j' caused by geometrical space γ, is specified by the geometrical factor $d_{i,j.}$ This is associated with the conception of "kink energy" (E_k) in equally spaced adjacent cells and this is often linked with the cost of energy between two QCA cells 'i' and 'j' having opposed polarization. It is computed as,

$$E_{i,j}=\frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_{i,n}q_{j,m}}{\left|r_{i,n}-r_{j,m}\right|} \quad (6)$$

At every cycle, the expectation energy value is calculated as

$$E=\langle H\rangle=\frac{\hbar}{2}\overline{\Gamma}.\vec{\lambda} \quad (7)$$

Here, the reduced plank constant is denoted as ħ, the coherence vector is denoted as $\vec{\lambda}$, and the energy associated with neighboring effects $\overline{\Gamma}$ is obtained as,

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$$\vec{\Gamma} = \frac{1}{\hbar}\left[-2\gamma, 0, E_k\left(C_{j-1} + C_{j+1}\right)\right] \quad (8)$$

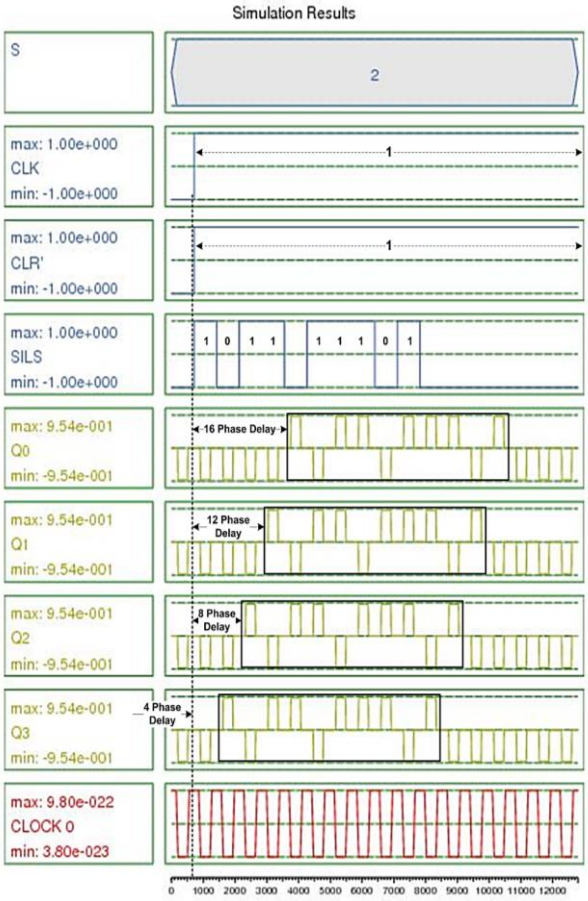

Figure 18. Simulated output of 4-bit CZBCUSR with S_0S_1='10' (SILS)

Power flow of QCA cell is classified into four main streams namely: (Input power 'I_P', Output power 'O_P', Clock power 'C_P' and Dissipation power 'D_P'. As reported in [42], the power of the horizontal signal (i.e) I_P and O_P are equal. I_P is the power obtained from the closest left cell and O_P is the power received from the closest right cell. Inter-dot barriers are gradually increased when in the switch phase, allowing large amounts of energy to be transmitted to the cell C_P. These obstacles are diminished moderately at the time of release phase and allow a portion of energy to be resorted to the clocking. As a result, insignificant energy dissipation is occurred in the clocking circuit and is called D_P. For a specific cell, the overall power factor can be measured as,

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right] = P_1 + P_2 \quad (9)$$

In (9), the term P_1 contains two core components: The first is the power gained from the difference of I_P and O_P and the other is the relocated C_P to the cell. In addition, the term P_2 stands for dissipated power D_P. The energy dissipation in a single clock cycle is calculated using coherence vectors and Hamiltonian matrix as follows,

$$E_{diss} = \frac{\hbar}{2}\int_{-T}^{T} \vec{\Gamma}.\frac{d\vec{\lambda}}{dt}dt = \frac{\hbar}{2}\left(\left[\vec{\Gamma}.\vec{\lambda}\right]_{-T}^{T} - \int_{-T}^{T} \vec{\lambda}.\frac{d\vec{\Gamma}}{dt}dt\right) \quad (10)$$

Most of the energy is dissipated at the rate of change of $\vec{\Gamma}$. As mentioned in [43], the upper bound power dissipation is taken into consideration for calculating maximum ($\vec{\Gamma}$+) and minimum ($\vec{\Gamma}$-) value. For QCA circuits, the above mentioned power dissipation model is developed in [21], by merging total power dissipation into two core components, namely: "leakage" and "switching". It is important to note that leakage power (E_L) is caused by power loss because of clock

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transitions (from minimum to maximum and maximum to minimum) and switching power (E_S) is caused by power loss because of cell switching states. For each input combination, the maximum, minimum and average power dissipation is calculated using QCAPro simulator tool [21] under "non-adiabatic" switching in different tunneling states. Besides that, according to Bayesian network evaluation, this can be used to verify the circuit's functionality.

A. Evaluation of energy dissipation in proposed structure

The dissipated energy of novel architectures such as multiplexer, D flip-flop, and Shift register implementation is measured using the power analysis tool QCAPro [21]. At temperature of 2 Kelvin, the dissipated energy for the proposed structure is investigated at 0.5 E_k, 1.0 E_k and 1.5 E_k tunneling energy levels. There are two distinct terminologies of energy dissipation namely, the leakage energy and switching energy dissipation, which emerged from cell switching state and clock transitions respectively. Using the concepts of non-adiabatic switching, the device measures the energy dissipation of each output combination in the entire circuit. The darker cell in map shows higher dissipation than the others.

Energy diagram of proposed 4 to 1 QCA MUX, novel D - flip flop and shift register is depicted in Fig. 19, Fig. 20 and Fig. 21, respectively at 2K temperature. "Switching energy dissipation" (SED), "leakage energy dissipation" (LED), and overall energy dissipation TED (SED+LED) are used to assess the proposed architecture's performance. Table 4, Table 5 and Table 6 summarizes the comparison results with the existing literature. At 0.5 E_k novel multiplexer configuration dissipates 84.18 meV, at 1.0 E_k it dissipates 108.94 meV and at 1.5 E_k it dissipates 139.43 meV as total energy dissipation, which is 36%, 31% and 37% lower than the existing literature. The novel D flip-flop configuration has 6.60 meV, 14.76 meV and 24.68 meV as total energy dissipation at different kink energy levels which is 33%, 41% and 40% lesser than the existing literature. Proposed shift register configuration has 102.97 meV, 185.41 meV and 266.13 meV as total energy dissipation at different kink energy levels. The energy dissipation of the proposed architecture is a smaller amount when compared to the literature.

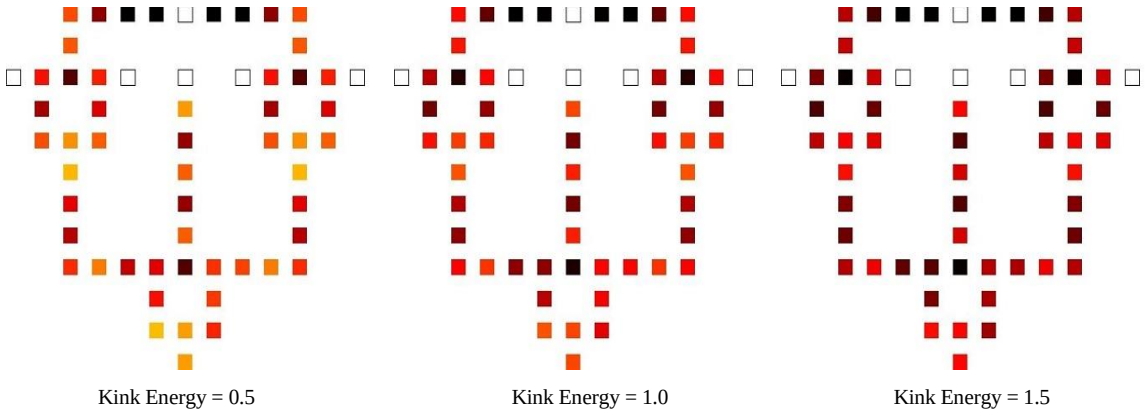

Figure 19. Energy diagram of 4 to 1 multiplexer for various Tunneling energy states

TABLE IV. COMPARISON OF ENERGY DISSIPATION BETWEEN THE PROPOSED MULTIPLEXER WITH LITERATURE

4 to 1 MUX	Average LED in meV			Average SED in meV			Total dissipation in meV (TED)=(LED+SED)		
	E_k@0.5	E_k@1.0	E_k@1.5	E_k@0.5	E_k@1.0	E_k@1.5	E_k@0.5	E_k@1.0	E_k@1.5
[10]	29.74	80.50	136.54	31.27	26.28	21.92	61.01	106.79	158.46
[11]	31.97	95.03	167.59	80.09	67.93	56.58	112.06	162.96	224.17
[12]	20.17	59.46	105.84	113.56	99.42	85.67	133.73	158.88	191.51
Proposed	18.81	53.72	93.190	65.37	55.22	46.24	84.18	108.94	139.43

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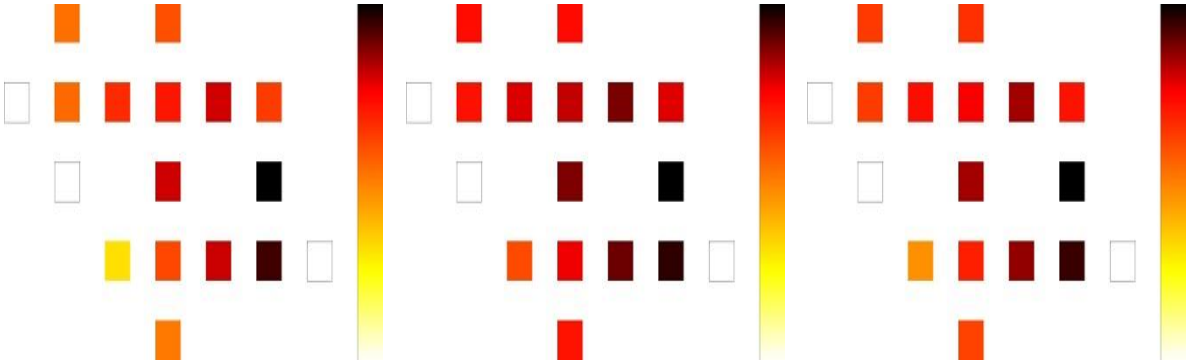
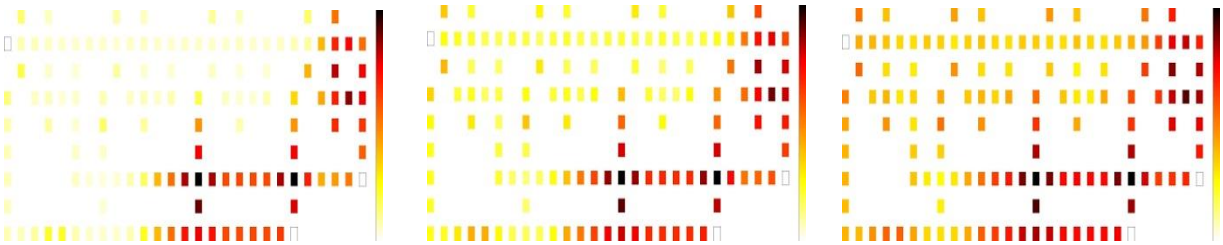


Kink Energy = 0.5 Kink Energy = 1.0 Kink Energy = 1.5

Figure 20. D flip-flop's energy diagram of various Tunneling energy states

TABLE V. COMPARISON OF ENERGY DISSIPATION BETWEEN THE PROPOSED D FLIP-FLOP WITH LITERATURE

D Flip-flop	Average LED in meV			Average SED in meV			Total dissipation in meV (TED)=(LED+SED)		
	E_k@1.0	E_k@1.5	E_k@0.5	E_k@1.0	E_k@1.5	E_k@0.5	E_k@1.0	E_k@1.5	E_k@0.5
[44]	10.27	31.52	56.47	48.50	41.68	35.18	58.78	73.20	91.65
[14]	3.86	3.09	3.86	18.57	52.95	90.92	22.43	56.04	98.19
[12]	7.78	22.49	39.13	2.21	1.82	1.57	9.99	24.30	40.71
Proposed	4.13	12.57	22.78	2.47	2.19	1.90	6.60	14.76	24.68



Kink Energy =0.5 Kink Energy =1.0 Kink Energy =1.5

Figure 21. Energy diagram of Serial in-Parallel Out Shift register for various tunneling energy states

TABLE VI. COMPARISON OF ENERGY DISSIPATION BETWEEN THE PROPOSED 4-BIT SHIFT REGISTER WITH LITERATURE

Shift Register	Average LED in meV			Average SED in meV			Total dissipation in meV (TED)=(LED+SED)		
	E_k@1.0	E_k@1.5	E_k@0.5	E_k@1.0	E_k@1.5	E_k@0.5	E_k@1.0	E_k@1.5	E_k@0.5
[40]	48.26	139.28	242.06	55.66	47.24	39.70	103.92	186.52	281.76
Proposed	31.46	101.55	191.17	71.51	83.86	74.96	102.97	185.41	266.13

6. QCA COST FUNCTION

In general, the cost function of any circuit is measured between area, delay and power consumption tradeoffs. In QCA circuit, the types of crossover is also included to measure the overall cost function. The generalized semiconductor QCA

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cost function is used in this paper, in which the number of Majority Gate (MG), Inverter (INV), Crossover (C) and delay (T), with various weights for each factor is included as metrics of evaluation. The evaluation of QCA cost function is expressed in (8) [20].

$$\left(MG^{\alpha} + INV + C^{\beta}\right) x\, T^{\gamma}, 1 \leq \alpha, \beta, \gamma \qquad (8)$$

Number of majority gates, inverters, crossover and delay in (8) are indicated by MG, INV, C and T respectively. The exponential weights for MG, C and T are α, β and γ respectively. The proposed and existing USR designs are implemented using majority gate, inverters and crossovers. In QCA cost function, the complexity in crossover, irreversible energy dissipation by majority gate and delay produced by the circuit were calculated as exponential factors. For evaluating the efficiency of high speed QCA circuits, delay is considered to be the primary concern. Due to arrangement of 45º rotated cells in coplanar crossover and precise three or five layer in multilayer crossover results in fabrication design complexity [8, 45]. The cost of multilayer crossing which is employed in [18] is thrice larger than the coplanar crossing. Whereas, CZBC uses regular cells to resolve these design complexities and it is formed between two completely different QCA wires with alternate clock zones [30]. None of the weight is assigned to the crossover (C) i.e β=0 [45], since the proposed USR is implemented using the CZBC technique. CZBC uses standard cells alone in QCA wires and it does not need rotated and multilayer QCA cells [28, 45]. Table 7 summarizes the QCA cost function of n-bit universal shift register with the literature and it shows that the proposed CZBCUSR has less cost function due to its lesser number of majority gate, inverter and delay. Furthermore, there is no crossover complexity in the proposed design due to clock zone-based crossover. A comparative metric is shown in Fig. 22 using (8). Based on Fig. 22, the proposed CZBCUSR have less cost compared to other QCA based USRs. In particular, the proposed CZBCUSR has around 32% 28% and 12% less design cost than the literature [10, 11 and 12] respectively. The major reason for obtaining this optimization is because of fewer majority gate utilization and CZBC technique for crossover. The proposed CZBCUSR design may extend for higher order bits.

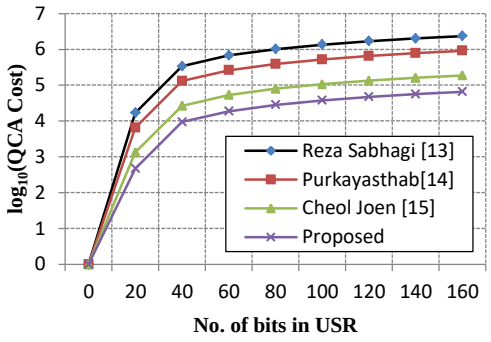

Figure 22. Comparison of USR with cost = $\left(MG^{\alpha} + INV + C^{\beta}\right) x\, T^{\gamma}$

7. PERFORMANCE COMPARISON

A performance comparison of the proposed architecture with respect to the literature is presented in this chapter. Table 8 presents a comparison towards the proposed QCA multiplexer with the existing architecture presented in [10, 12] and [16, 36, 46]. Number of QCA cells is reduced by 10% in the proposed 2 to1 multiplexer, which is used to design 4 to 1 multiplexer. In 4 to 1 QCA multiplexer, the number of QCA cells is minimized around 40%, when compared with the literature and in terms of delay [12] achieves 4 phase clock delay but the proposed design achieves 3 clock phase delay this in turn reduces 25% of overall latency. Table 9 presents a comparison of D flip-flop with literature. The proposed D flip-flop has 17 cells and it occupies 0.02 μm^2 area as well as three clock phase delay and the CLR' input is attached in the proposed D- flip flop to reset the circuit at any time. The proposed design cell count is minimized up to 29% and the latency is reduced up to 25% than the recent literature. Among the literature [13] consumes a larger area as 0.70 μm^2, due to coplanar crossover, which normally increases the area than the other crossovers. Comparison of shift register is shown in Table 10. Shift register proposed in [11, 12] does not have a reset ability. Therefore, those circuits have higher latency than the other architectures. Proposed shift register has better efficiency compared to [40] with reset ability.

TABLE VII. SUMMARY OF N-BIT UNIVERSAL SHIFT REGISTER COST FUNCTION

n-Bit USR	No. of MGs	No. of INVs	Number of Crossings	Delay in Clock cycles	QCA Cost $\left(MG^{\alpha} + INV + C^{\beta}\right) x\, T^{\gamma}$

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[10]	10n	4n	-	8n+7	$(10n^{\alpha} + 4n)\ x\ (8n + 7)^{\gamma}$
[11]	9n	4n	n ($\log_2$ n-3) + $\log_2$ 2n +2	4n	$\left(9n^{\alpha} + 4n + (n(log_2\ n - 3) + \ log_2\ 2n\ + 2)^{\beta}\right)\ x\ 4n^{\gamma}$
[12]	2n	6n	2n ($\log_2$ n-1) + 4n +2	3n+1	$\left(2n^{\alpha} + 6n + 2n(log_2 n - 1)_{4n} + 2^{\beta}\right)\ x\ (3n + 1)^{\gamma}$
CZBCUSR	3n	2n	-	n	$(3n^{\alpha} + 2n)\ x\ n^{\gamma}$

Eventually, when in comparison of the proposed CZBCUSR with yet another QCA based USR, in terms of circuit complexity, area and delays is depicted in Table 11. From this Table, it is noticed that the proposed design is lowered by 38% in cell count and the latency is minimized by 69%. Because of reduction in number of cells and latency, area delay product of the novel design is also reduced. Among all the universal shift registers, the proposed CZBCUSR has the reset ability feature to reset the circuit at any time. Due to this feature, proposed design achieves lesser delay than the existing designs.

TABLE VIII. COMPARISON BETWEEN MULTIPLEXERS WITH LITERATURE

2 to 1 Mux	Complexity (Cell Count)	Area in μm^2	Delay (Clock Phase)	Area Delay Product
[10]	26	0.02	2	0.04
[12]	13	0.01	1	0.01
[16]	15	0.01	2	0.02
[17]	16	0.01	2	0.02
[46]	17	0.01	2	0.02
Proposed	12	0.01	1	0.01
4 to 1 Mux	Complexity (Cell Count)	Area in μm^2	Delay (Clock Phase)	Area Delay Product
[10]	161	0.24	35	2.1
[11]	101	0.11	5	0.55
[12]	69	0.08	4	0.32
[13]	139	0.25	9	2.25
[17]	73	0.06	8	0.48
Proposed	58	0.07	3	0.28

TABLE IX. COMPARISON BETWEEN "D FLIP-FLOP" WITH LITERATURE.

D Flip-Flop	Complexity (Cell Count)	Area in μm^2	Delay (Clock Phase)	Area and Delay Product	Reset Ability
[10]	52	0.06	6	0.36	No
[11]	48	0.03	3	0.09	Yes

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[12]	24	0.02	4	0.08	No
[13]	43	0.70	5	3.50	Yes
[14]	53	0.04	9	0.36	Yes
[15]	24	0.02	4	0.08	No
Proposed	17	0.02	3	0.06	Yes

TABLE X. COMPARISON BETWEEN SHIFT REGISTERS WITH LITERATURE

Shift Register	Complexity (Cell Count)	Area in μm^2	Delay (Clock Phase)	Area and Delay Product	Reset Ability
[11]	256	0.28	8	2.24	No
[12]	140	0.16	6	0.96	No
[40]	138	0.12	4	0.48	Yes
Proposed	132	0.11	4	0.44	Yes

TABLE XI. COMPARISON OF PROPOSED CZBCUSR WITH OTHER QCA BASED USR.

USR	Complexity (Cell Count)	Area in μm^2	Delay (Clock Phase)	Area and Delay Product	Reset Ability
[10]	1954	3.06	37	113.22	No
[11]	1286	1.59	16	24.44	No
[12]	1048	1.04	13	13.52	No
Proposed	705	0.70	4	2.8	Yes

CONCLUSION

Novel multiplexer and D flip-flop configuration are employed to realize the proposed clock zone-based crossover universal shift register (CZBCUSR). A novel 2 to 1 multiplexer is designed by applying the inherent logical characteristics of quantum dot cellular automata by avoiding the existing majority gate and inverter design. This aids to lessen the number of cells and area in the proposed architecture. An optimal 4 to 1 multiplexer is designed by exerting three 2 to 1 multiplexers. A simple inverter with CLR' input aids in constructing the proposed D – flip flop. CLR' input is used to reset the register prior to its clock operation which, brings down the circuit latency drastically. The coplanar and multilayer crossover has fabrication difficulties and it simultaneously increases the overall cost of the circuit, which is fixed by the clock zone-based crossover in the proposed architecture. The simulation result shows that the cost of the proposed CZBCUSR is comparatively better than the earlier design due to lesser number of majority gate, inverters and delay consumption. The proposed CZBCUSR is utilized for data transfer and data manipulation circuits. Furthermore, this work could generalize the model of n-bit universal shift register.

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