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Effect of Etching Time on the Topography of Porous Silicon Surfaces Produced by Electro Chemical Method

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ABSTRACT:

This study includes the effect of etching time(5-10-15)minon morphology of porous silicon surfaces which density applied (30) mA and constant concentration (1:9) methanol : HF.

The production of Nano crystalline silicon structures and control of their production conditions is the first step to control the properties of the devices (detectors, diodes, solar cells, sensors) and their appropriate applications. Ultimately, this is important in promoting research and development of renewable energy , We observe this study that the roughness , average diameter and root mean square are increasing with increasing the etching time of silicon wafers, and these results are agreement with [1] , [2] .

Keys to search are:

The etching, roughness, porous silicon, electrochemical etching, quantum confinement.

1.Introduction

The porous silicon wafers may be used to producedetectorsand diodes, whenthe bulk siliconetching , the area of the surface it will be larger than the area of the surface before etching that increase their efficiency and increasing the surface area of the solar cell for example. There are methods to manufacture a nanoscale size of the material,porous surfaces with nanoscale dimensions such as the photochemical method and electro-chemical method[3].

In this work we used the electrochemical method, which is one of the important methods of producing a porous layer on the silicon wafer by using athe silicon wafers, Teflon Cup (acid-resistant material) and the wafers are immersed in the HF hydrofluoric solution and at a certain
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2.Theoretical part

2.1The surface morphology

The structural properties of n-type porous silicon (PS) prepared by theelectrochemical etching , are investigated by AFM, technique, The surface topography of the material is important to explain the properties and behavior of the material. Nanomaterial's are different from other conventional materials by increasing the surface area and the presence of most of their atoms on these surfaces because all chemical and physical activities and changes always occur on the surface. the topography study shows how the atoms are distributed on the surface . [4]

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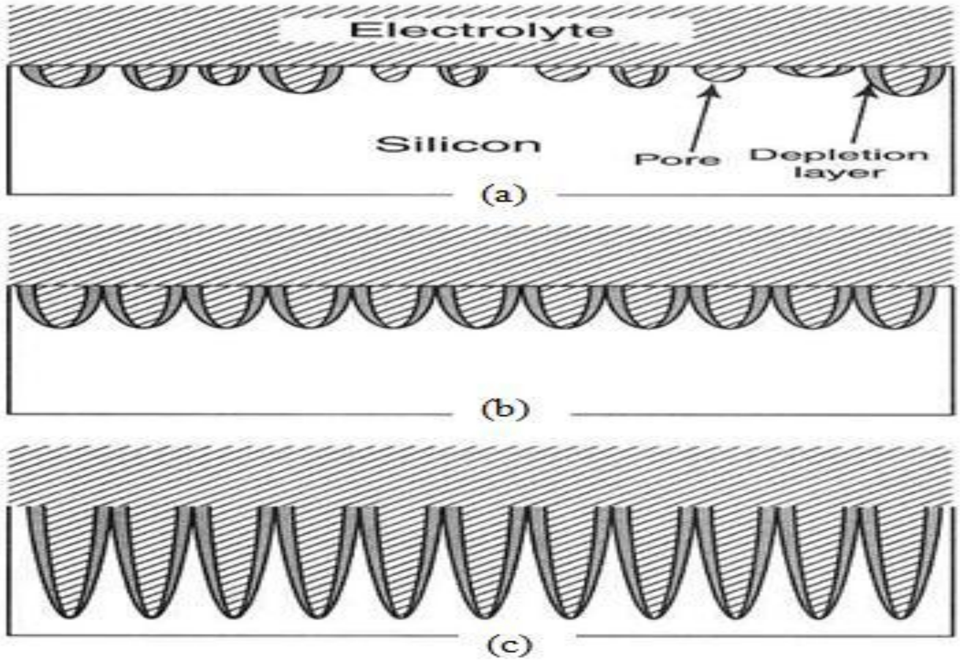

Figure (1): Pore formation in porous silicon. (a) The initial stage, where the pores created randomly on the wafer silicon surface. (b) The depletion zones around each pore overlap, the pore growth changes to a highly directional growth (c) Only at the pore tips the dissolution occurs [5].

2.2 Nano porous silicon

The development of porous silicon gave a new dimension to thetechnologies,which based on porous silicon, in 1990 and the discovery of photoluminescence at room temperature of porous silicon by Canham [6], did not use bulk silicon in the field of light sources (LED) , Because silicon is a semi-conductive material with an indirect band gap semiconductor, and therefore the light fluorescence occurs at room temperature very small [6,7].

Researchesare currently focused extensively on the study of the properties of nano-porous silicon as a luminesce material. The importance of porous silicon is not limited to photovoltaic applications but depends on its properties as a crystal with a bright light [8], which changes the optical properties and absorption, optical reflectivity, making it sensitive to specific wavelengths and useful in optical applications. By controlling the etching conditions (time, slide specification, acid concentration) so that a suitable crystalline structure for porous silicon nanoparticles can be obtained with different porous layers. The importance of using porous silicon nanoparticles in the manufacture of photoconductor and diodes and their properties Especially in terms of industrial use compared to other materials used in this field of low cost of manufacture and the possibility of preparing the surface for high selectivity [9] as well as the provision of raw material and the lack of energy loss due to the small size of manufacturing.

2.3 Porous Silicon Formation Methods

Several methods are used and developed to fabricate the porous layerwith wide variation of pore morphologies having the pore dimensions frommicro to nanometers. There are five important methods for fabricating PSlayer [5]:

☐ Photochemical.☐ Electrochemical.☐ Photo-electrochemical.☐ Stain etching processes.☐ Laser Induced Etching Process.

The most common among them are the stain etching and theelectrochemical etching of the silicon wafer.

Electrochemical Method: .3.12

In this studywe used electrochemical etching to produce porous silicon layer. The time etching which is the different item of the electrochemical method , and some things ,like electrolyte .

The p-type silicon wafer were selected with (111) to study the effect of etching time on the topography of the surfaces which is poroused.

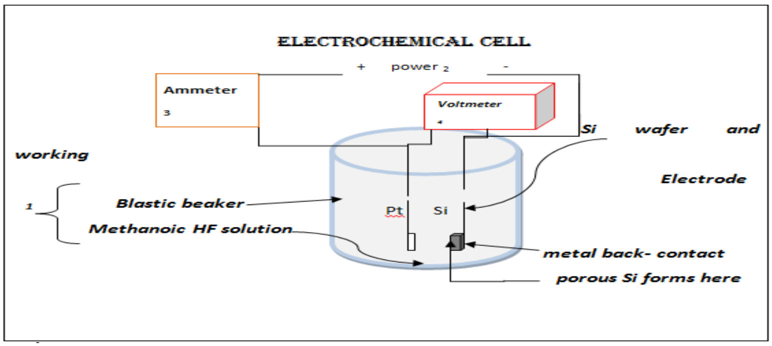

Figure (2): Schematic of the designed porous silicon fabrication system(electrochimcal cell)[2].

After cleaning the silicon sample, it is immersed in electrolyteFig.(2). We changed thetime of etching among (5-10-15) min with constant concentration of electrolyte and current density(30)mA, after that and when the process was ended we can see the effect of etching time on porous silicon surfaces by using the AFM investigate .

3 . Experimental part:

The P-type silicon wafers were selected with 111 orientation to study the effect of etching time on the topography . cleaning the samples with acetone and ethanol to remove the suspended materials and then put them in HF and 10% concentration for 15 seconds to remove the oxide layer usually on the silicon surface.`

After cleaning the silicon samples, they are immersed in electrolyte with concentration (9:1) HF and chohole respectively inside a teflon cup based on the same Teflon material Fig.(2). In this way the holes moving to the surface (positive charges) Fig. (3).

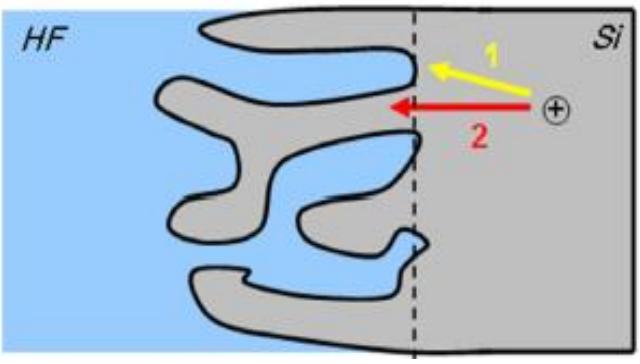

Figure (3) the corresponding band diagrams forcharge transfer(1) from thebulk to the electrolyte in the pore tip are presented (2) from the bulk to the porous silicon [4].

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3.1AFM of morphology for samplesurfaces produced by the electrochemical method

The samples were selected p-type ,resistivity (ρ= 1-4) Ω. Cm anddirectional (111) and the magnification time (5-10-15 min) were performed under conditions (1:9) electrolyte concentration and intensity of current (30) mA to study the difference in Morphologyon the produced porous layer.

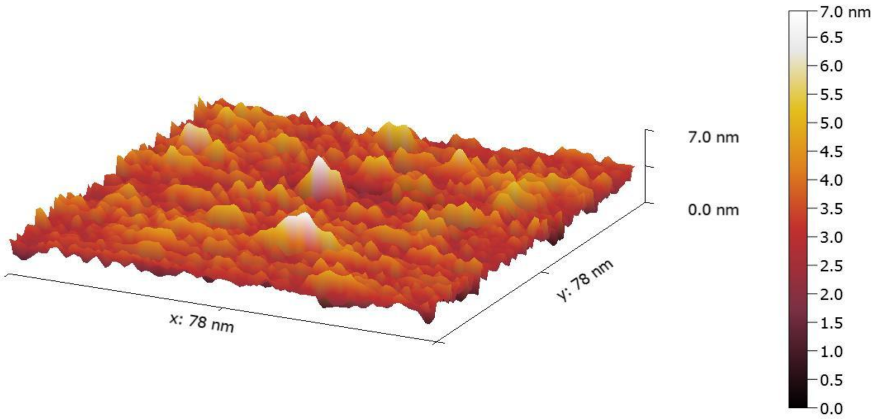

Figure (4): AFM image of PS surface at constant current density 30mA/cm^2 and at 5minetching time for p-type silicon wafer.

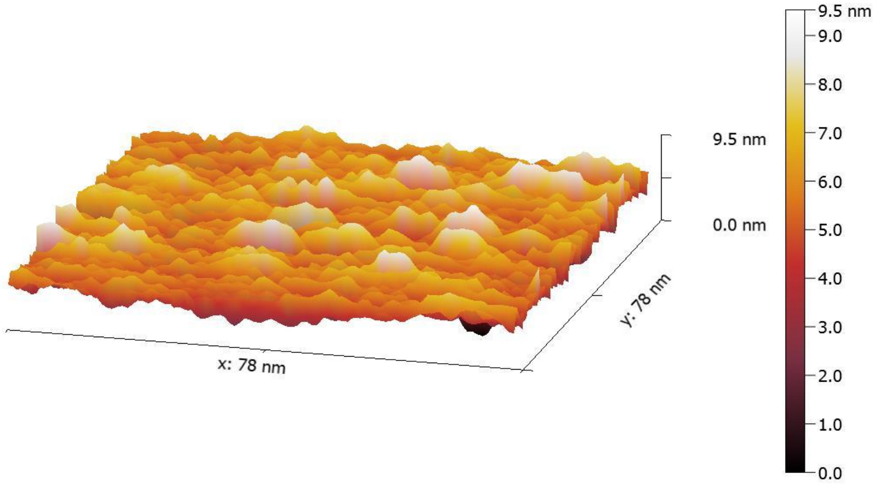

Figure (5): AFM image of PS surface at constant current density (30)mA/cm^2 and at (10)minetching time for p-type silicon wafer.

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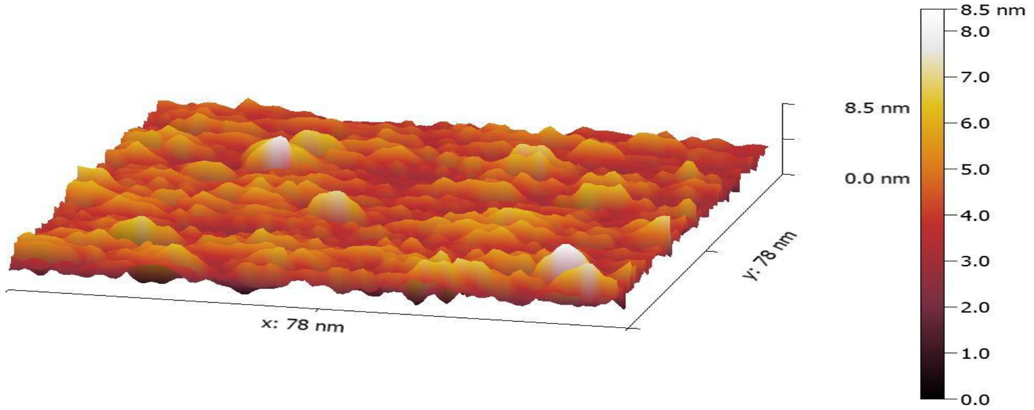

Figure (6): AFM image of PS surface at constant current density (30)mA/cm^2 and at(15) min etching time for p-type silicon wafer.

Table (1): Some properties of surface morphology which produced by electrochemical method .

Current density($mA\ cm^{-2}$)	Time anodization (min)	Si-type	height PSLayer (nm)	root mean square nm)(	Avg. diameterm (nm)
30	5	P	23	4.2	82.71
-	10	-	44	6.9	109.45
-	15	-	60	12.2	132.36

4.Results and Discussion:

In this part of the research, the Atomic Force Microscope (AFM) was studied and analyzed by studying the shapes and sizes of the formed nanoparticles, most of which ranged from less than (100nm), which are within the dimensions of nanotube particles, As well as the results of the atomic forcemicroscope is conclusive because of the richness in the information it provides such as average roughness and the value of the average root square object (Root Mean Square) and the distance between Peak-Peak and a lot of information on which the characteristics of manufactured devices can be explained. As mentioned in the above items, the work is focused in Study of the effect of etching time on the topography of the porous silicon surface produced when all the conditions of the endoscopy itself (3-1) conclude from figures (4 , 5 , 6) and Table (1) that the surface roughness increases as the time increasing , The crystalline structures on the surface are reduced by the increase in the process of formation, where erosion and scraping is not confined to the depth, but there is also a etching on the walls and grooves produced by electrochemical etching. We also note that the thickness of the porous layer of the etched simple under the etching was increasing with increasing time of etching , because the continuation of drilling and colonization were continues in uproot with same directetching in depth.

5.Conclusions:

1- The porosity layer increased in the silicon wafer surfaces by increasing the etching time , where the movement of the carriers continues, which leads to increasing in the porosity.
2- The etching method has affected the porosity, The porosity layer increased in the silicon wafer surfaces by electrochemical method , because the current of the curriersfrom the far side to the opposite side, which leads to increase the etching processes in the surface of the wafers.

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3- From the three pictures we conclusion that, aA the etching time increases, the sharpening of the productive Summits decreases.

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