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Quadrature Amplitude Modulation Using Booth Multiplier with Area Efficient for Network on Chip

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ABSTRACT

The design key factors of the VLSI (Very Large-Scale Integration) are the power and delay. In this proposed method, n-Quadrature Amplitude Modulation is preferred for Booth Multiplication in network applications. Among various types of digital modulation schemes, the choice of Quadrature Amplitude Modulation is to provide both phase and amplitude modulation. The use of n-Quadrature Amplitude Modulation is to overcome the drawbacks in other types. The output and the bit rate depending on the value of n. This is efficient when compared to Quadrature Phase Shift Keying by reducing power consumption and increases the area efficiency and bandwidth. The coding is converted to Verilog HDL. Xilinx is responsible for the simulation and synthesis part of this work.

KEYWORDS

Area Efficiency, Power Consumption, Xilinx.

Introduction

In this research we achieve improved processing capability, various reconfigurable multiplier techniques have been developed that can support multiple precision multiplications. There have been several researchers who have paid attention to solving timing problems, in particular, thus building a complete communication system. This article presents a complete design of a VHSIC-HDL, Very High-Speed Integrated Circuit Hardware Description Language (VHDL) based 16-QAM transmitter and receiver. This system can be used in a typical WiMAX system and any other QAM based communication system.

Proposed Work

a) Quadrature Amplitude Modulation (QAM)

QAM permits an analog signal to with efficiency transmit digital info and will increase usable information measure. Phase modulation (analog PM) and section shift secret writing (digital PSK) is thought of a special case of QAM, wherever the amplitude of the transmitted signal could be a this will additionally touch modulation Frequency Modulation (FM) and frequency shifting secret writing (FSK) victimization construction Amplitude Modulation (AM). In QAM, the constellation points area unit is sometimes organized in a very sq. grid with equal vertical and horizontal spacing, though alternative configurations area unit potential. By switch to a higher-order constellation, a lot of bits per image is transmitted it's a multi-carrier digital modulation theme that extends the construct of modulating one sub-carrier by victimization multiple sub-carriers inside an identical signal channel.

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b) Proposed Block Diagram of QAM Modulator

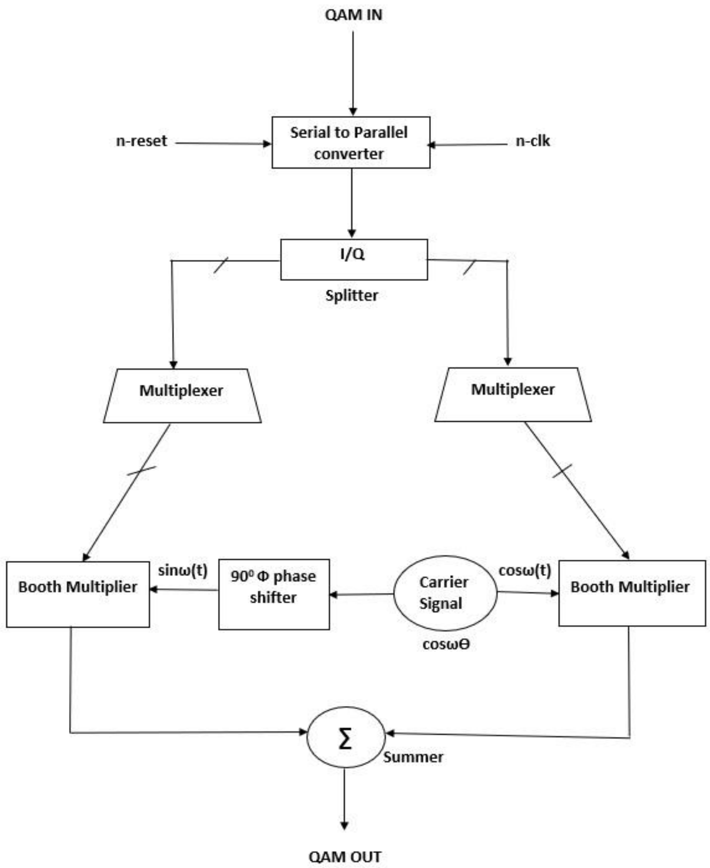

Figure 2.1. Proposed Block Diagram of QAM Modulator

c) QAM Modulator

Figure 2.1 shows the proposed block diagram in which the QAM I/P is given first to the serial to the parallel converter with n-reset and n-clk to the I/Q, which has a splitter with in-phase and quadrature-phase. This passes through the multiplexer to the booth multiplier. In the booth multiplier 90^0 phase shifter of the carrier signal. Finally, it reaches the summer, and QAM output is being received.

d) Constellation Diagrams

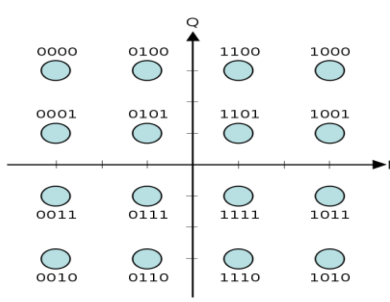

Figure 2.2. 16-QAM Constellation

Figure 2.2 represents 16-QAM constellation points with all points having 4-bits representation. Decision boundaries for 4-QAM are long-distance where 16-QAM is so small.

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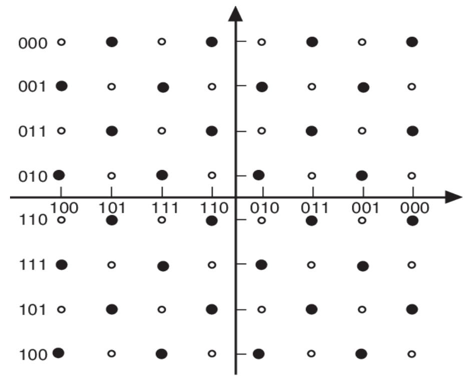

Figure 2.3. 32-QAM Constellation

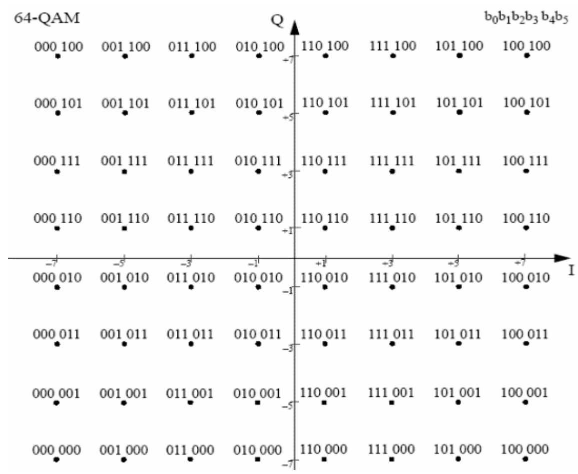

Figure 2.4. 64-QAM Constellation

Consequently, tiny amounts of noise will cause larger issues. because the background level will increase thanks to the low signal strength, the realm coated by a constellation purpose will increase. Also, because the amplitude variation will increase, the potency level decreases. this can be important for the battery potency of the mobile instrumentation and also the energy potency of the bottom station.

e) Bits Per Symbol

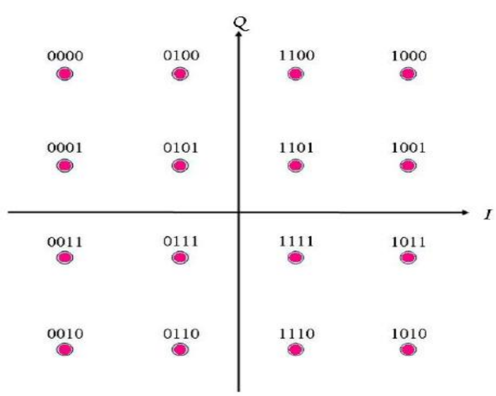

Figure 2.5. The bit mapping for 16-QAM

The figure 2.5 shows the QAM bit mapping in the case of 16-QAM with the values highly considered in the bit mapping for bits per symbol.

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f) Quadrature Amplitude Modulator Basics

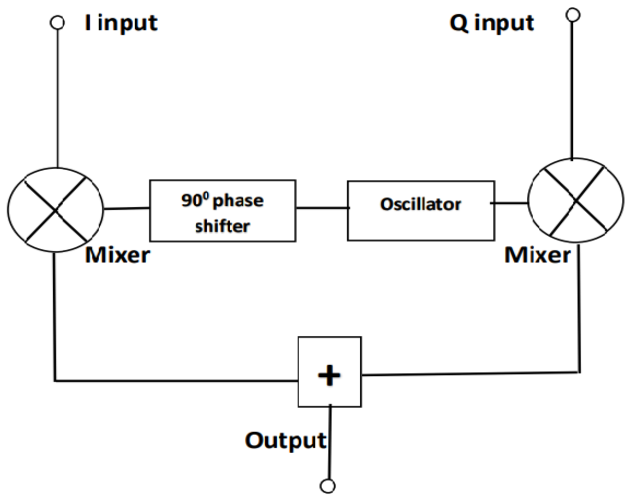

Figure 2.6. Basic QAM I-Q Modulator circuit

Figure 2.6 shows the block diagram of the proposed QAM modulator in which the QAM input is given first to the mixer to the I/Q, which has a splitter with in-phase and quadrature-phase. This passes through the multiplexer to the booth multiplier. In the 90^0-phase shifter of the carrier signal. Finally, it reaches the summer, and QAM output is being received.

g) Booth Multiplier

Booth Multiplier was found to be able to efficiently disable ineffective circuits that did not produce an effective result, thus operating speed is increased.

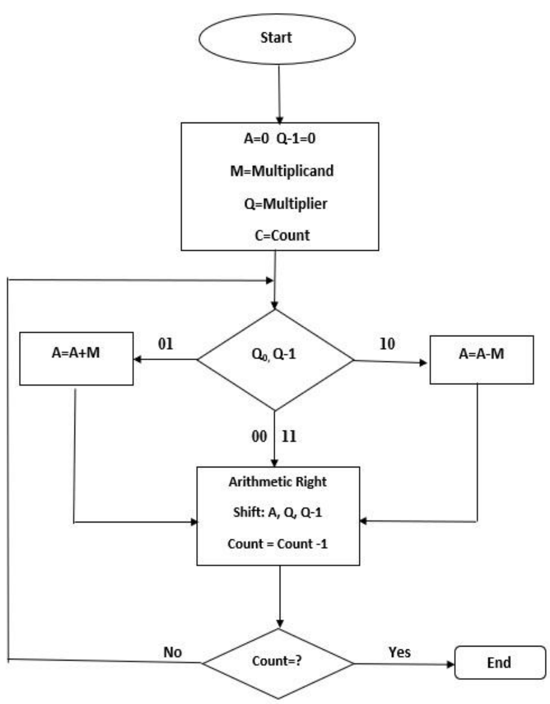

Figure 2.7. Flow chart of Booth Multiplier

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And so, that's where Booth's algorithm comes to the rescue. The Booth algorithm maintains the mark of the result. When 3 consecutive bits are equal, the add / subtract operation can be skipped. However, the performance of the stand multiplier for delays depends on the given data.

h) Booth Multiplication

Booth's algorithm for binary multiplication example is given below.

- Multiply 14 times -5 using 5-bit numbers (10-bit result).
- 14 in binary: 01110
- -14 in binary: 10010 (so we can add when we need to subtract the multiplicand)
- -5 in binary: 11011
- Expected result: -70 in binary: 11101 11010

Table 2.1. Comparison of various multipliers

Step	Multiplicand	Action	Multiplier Upper 5-bits 0, Lower 5-bits multiplier, 1 "Booth bit" initially 0
0	01110	Initialization	00000 11011 0
1	01110	10: Subtract Multiplicand	00000+10010=10010 10010 11011 0
		Shift Right Arithmetic	11001 01101 1
2	01110	11: No-op	11001 01101 1
		Shift Right Arithmetic	11100 10110 1
3	01110	01: Add Multiplicand	11100+01110=01010 (Carry ignored because adding a positive and negative number cannot overflow) 01010 10110 1
		Shift Right Arithmetic	00101 01011 0
4	01110	10: Subtract Multiplicand	00101+10010=10111 10111 01011 0
		Shift Right Arithmetic	11011 10101 1
5	01110	11: No-op	11011 10101 1
		Shift Right Arithmetic	11101 11010 1

Table 2.1 shows the booth's algorithm for binary multiplication example.

i) Booth Multiplier Architecture

Figure 2.8 shows the diagram of Booth's multiplier that multiplies two 16-bit numbers in at the value of two's

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complement.

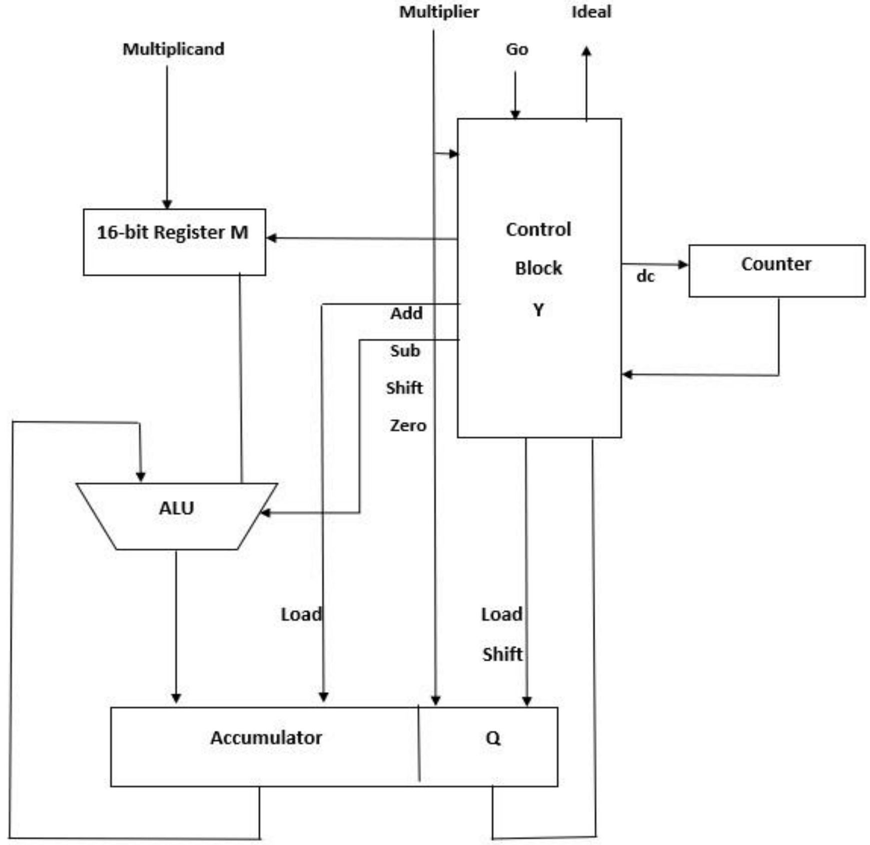

Figure 2.8. Architecture of Booth Multiplier

The architecture of booth multiplier has a 16-bit register with arithmetic and logic unit with an accumulator. The operations such as Add, Subtract, Shift also are given as input for the control block.

Results and Discussion

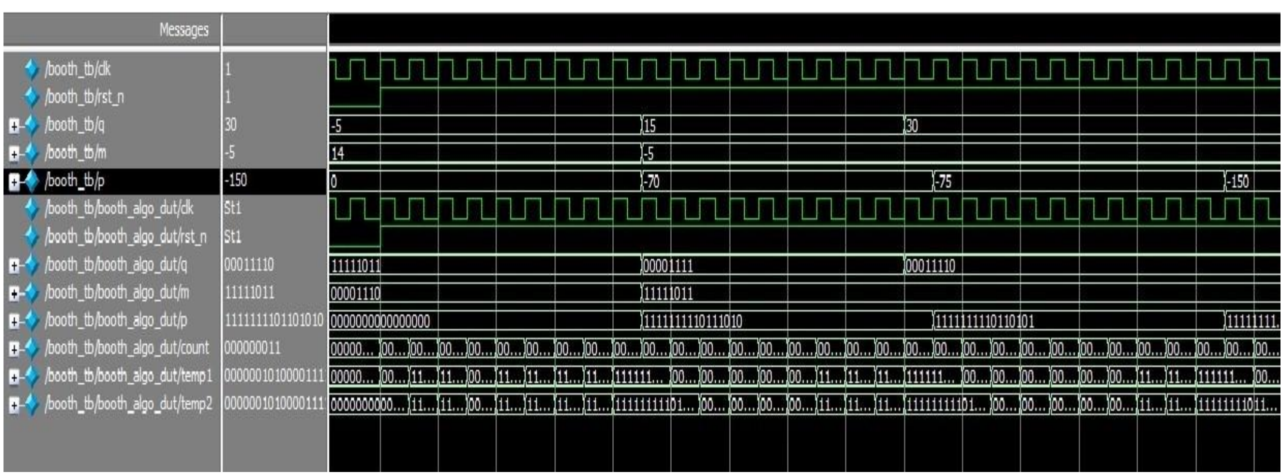

Figure 3.1. Booth Multiplier wave

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Figure 3.1 shows the various waves for the input given to the booth multiplier.

Figure 3.2. Booth Multiplier wave with values

Figure 3.2 shows the various inputs in the signed decimal form of the booth multiplier.

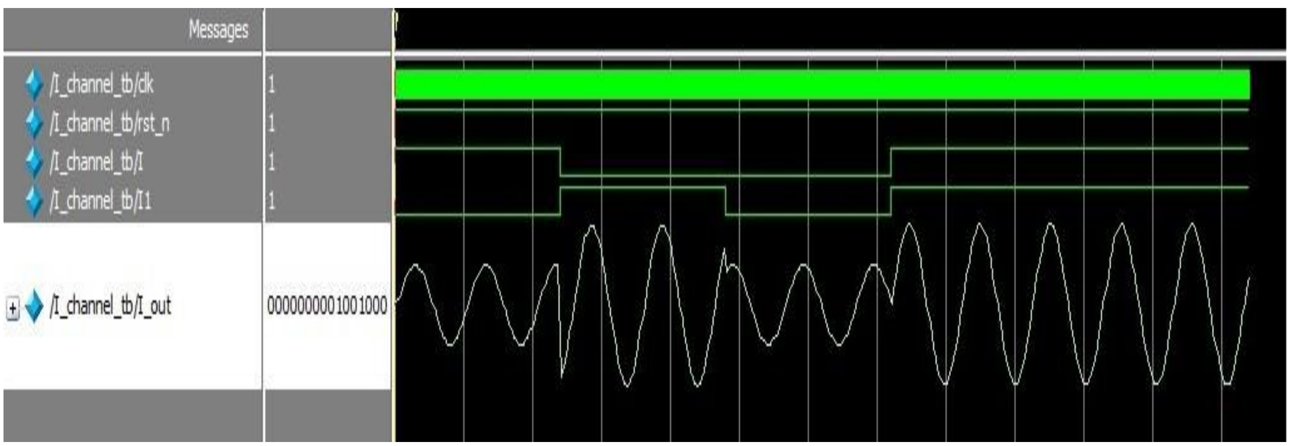

Figure.3.3. Output wave of the I channel

Figure 3.3 shows the various sin waves for the input bit values for the Inphase channel.

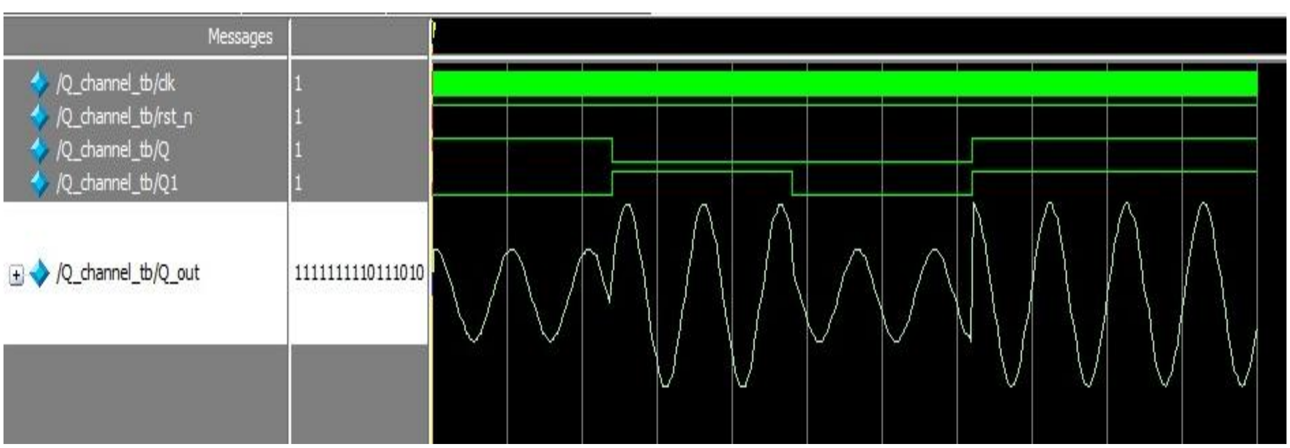

Figure 3.4. Output wave of the Q channel

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Figure 3.4 shows the 90^0 phase-shifted cos waves for the input bit values for the Quadrature channel.

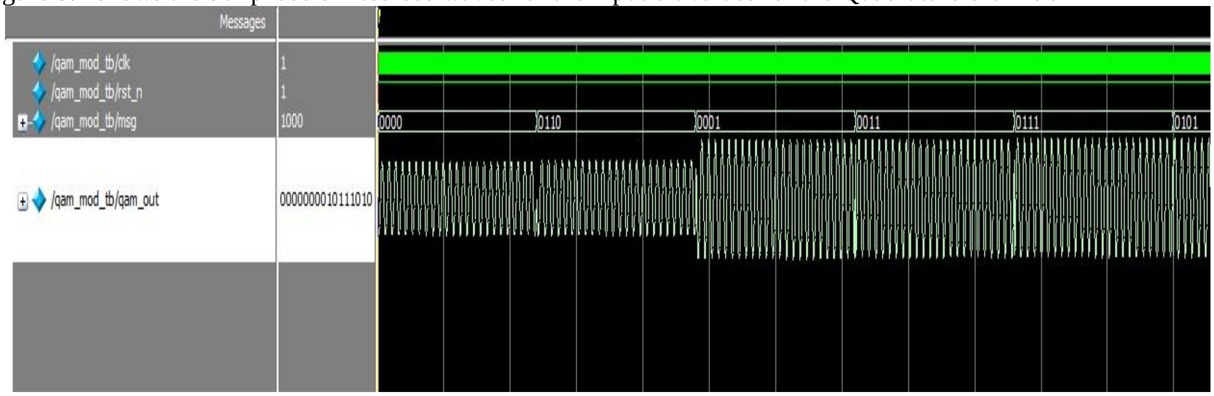

Figure 3.5. QAM modulator wave

Figure 3.5 shows that the two resultant signals are summed and then processed as required Figure 3.5 shows that the two resultant signals are summed and then processed as required in the RF signal chain.

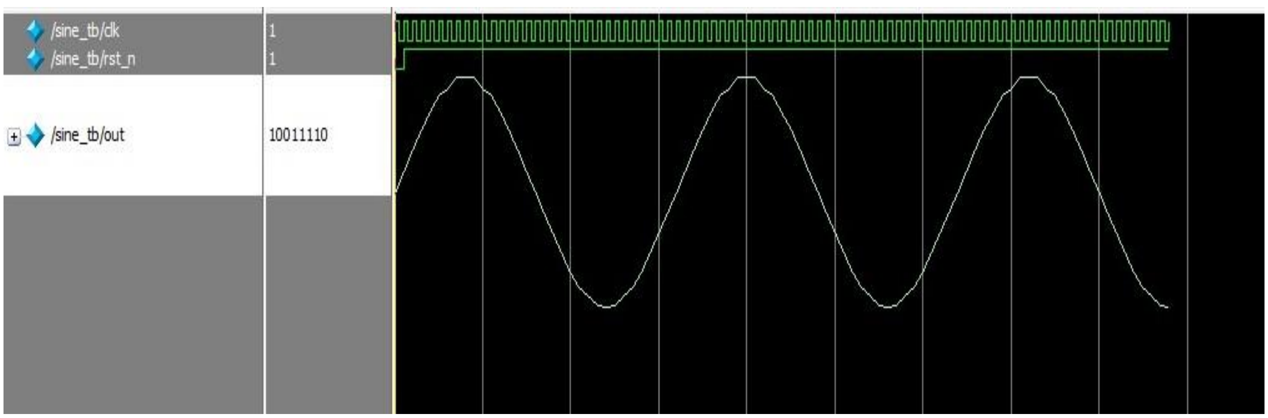

Figure 3.6. Sin wave generator

Figure 3.6 shows the sine wave of the sine wave generator with the input clock.

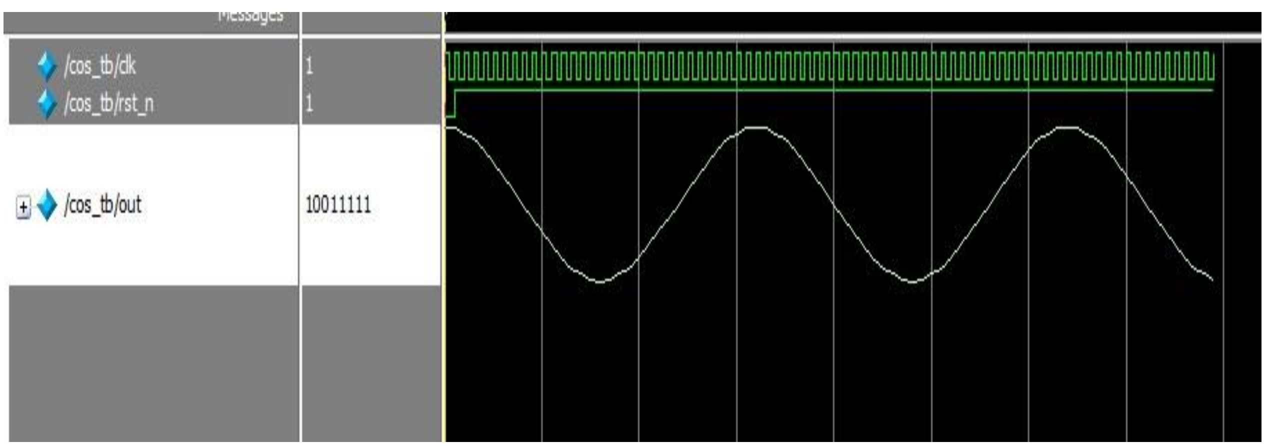

Figure 3.7. Cos wave generator

Figure 3.7 shows the cos wave of the cos wave generator with the input clock

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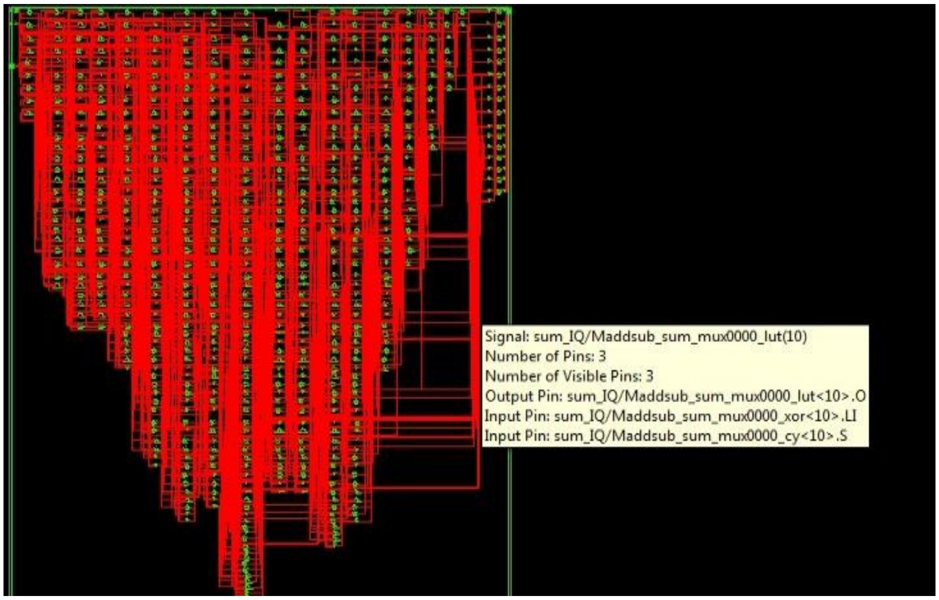

Figure 3.8. Technical View

Figure 3.8 is the process of converting a network of technology independent logic gates into a network comprising logic cells on the target FPGA device.

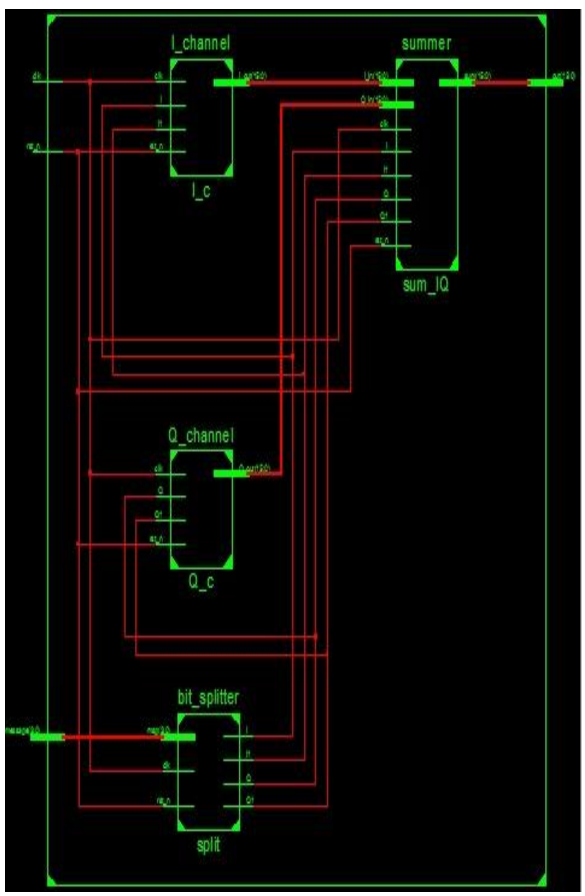

Figure 3.9. RTL View

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Figure 3.9 shows the Register-Transfer Level (RTL) which is a design abstraction model.

Conclusion

When we compare the QAM and PSK they are very good in the case of area, bits per symbol and bandwidth efficiency. In the comparison of noise immunity, it is better in QAM when compared to PSK. QAM has far better transmission power. For some noise immunity, 16-PSK required 1.6 dB higher power compared to 16-QAM. Here we use QAM because they have both amplitude modulation and phase modulation where PSK has only phase modulation. It is difficult to have amplitude modulation at high-frequency. QAM is more immune to noise. By increasing the distance from the centre point noise immunity can be increased, at low transmitting power.

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