Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 17874 - 17880
Received 25 April 2021; Accepted 08 May 2021.

Low Power Digital Lock Detector Using Gating D Flip Flop

Vamshi Krishna Raj.S[1*], Vishnu Priya.G[2]Venkata Sai Krishna.L[3]Nagarjuna Malladhi[4*]
[1,2,3,4] Department of Electronics and Communication Engineering, Vardhaman College of Engineering
Hyderabad, INDIA-501218.
*samsettyvamshi35@gmail.com, malladhinagarjuna@vardhaman.org

ABSTRACT

This paper talks about the optimization of a digital lock detector for dual loop PLL. The dual loop consists of fine tuning and coarse tuning. In a conventional digital lock detector, D flip flops are used. In this paper we have replaced these D flip flops with the gate clocked D flip flops. The digital lock detector is mainly used to detect frequency variations during the operation of a digital filter of the given detector. The digital lock detector is used between these PLL's for obtaining the frequency lock information to another PLL loop. Here we were able to decrease the output dynamic power by 12.31 mW, which is quite considerable.

Keywords

Digital lock detector; D flip flops; Clock circuit; Dual loop PLL

Introduction

As the name suggests, a digital lock detector detects when the reference signal and the feedback signal are of the same frequency. It consists of two n-bit counters, the former counts the number of 1's in a reference signal, and the later counter counts the 1's in the feedback signal. Thus, if this count values are equal then the lock condition is established. Therefore in [4], a lock signal indicates that the reference and the feedback signal are of the same frequency

In [7], the dual loop PLL consists of fine PLL and coarse PLL, the coarse PLL is used for faster convergence whereas the fine PLL is used for fine tuning. The dual loop PLL is applied to digital lock detector to verify it [2]. The dual loop structure is used to increase PLL locking speed and decrease phase noise in the circuit

The gated D flip flop is a single input methodology which is used either to set or reset the flip flop. When the gate in the flip flop is high, the output follows the input. When the gate in the flip flop is low the gated D-flip flop gets latched. It is one of the widely used technology to reduce the dynamic power dissipation. It is mainly used in the synchronous circuits where the clock circuit is turned off when the signals are synchronous to each other. Thus, by this method we are removing the clock circuit when it is not necessary. We avoid the change in states in the D flip flops and thus we can avoid the unnecessary switching activity.

This idea is very worth these days, because a digital lock detector is widely used in the NFC (Near field communication) technology. As wireless mode of transactions and communications is the future. Here we discuss the combination effect of the gate clocking method to the existing digital lock detector and observe its effects and try to draw the conclusion from it. Further, we see the review of the papers that helped to write this paper and later, we see the existing and the proposed methodology. Finally, we see the results and conclusions.

Literature Review

In [2], a brief description of the digital lock detector was proposed. It uses a digital lock detector between the coarse PLL and the fine PLL. The lock detector conveys the locking information to the fine PLL which ensures that the lock is established and further communication takes place. It uses 0.13 μ-m CMOS technology and uses 1.2 V DC power supply. It studies the frequency variations under different locking conditions and deduces the locking condition and criteria.

In [1], power consumption of a D flip flop is shown. The optimization is done using the Gate diffusion technique using the gate clocking technology. A significant optimization of 1.38% was achieved using this technique. The Gate diffusion technique was used because it has the lowest power delay product as compared to other CMOS configurations. An in detailed study of various types of D flip flops was studied along with its pros and cons. Thus, after analyzing all these, the above-mentioned optimization of 1.38% was achieved.

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 17874 - 17880
Received 25 April 2021; Accepted 08 May 2021.

The principle of phase locked loop is the primary principle in the working of any digital lock detector, even a single-phase locked loop is sufficient but the advantage of dual phased lock loop is used to increase the precision of the phase locked loop.

A clear understanding of the phase locked loop is given in [7]. Also, the importance of delay and how it can be implemented with the D flip flops that we used can be understood by studying the delay locked loops in [5].

In [3] a clear overview of the older version of the digital lock detector is used in which the error detection techniques were not use this was over came by introduction of an error detector circuit in the existing technology given in [6].

Existing Methodology

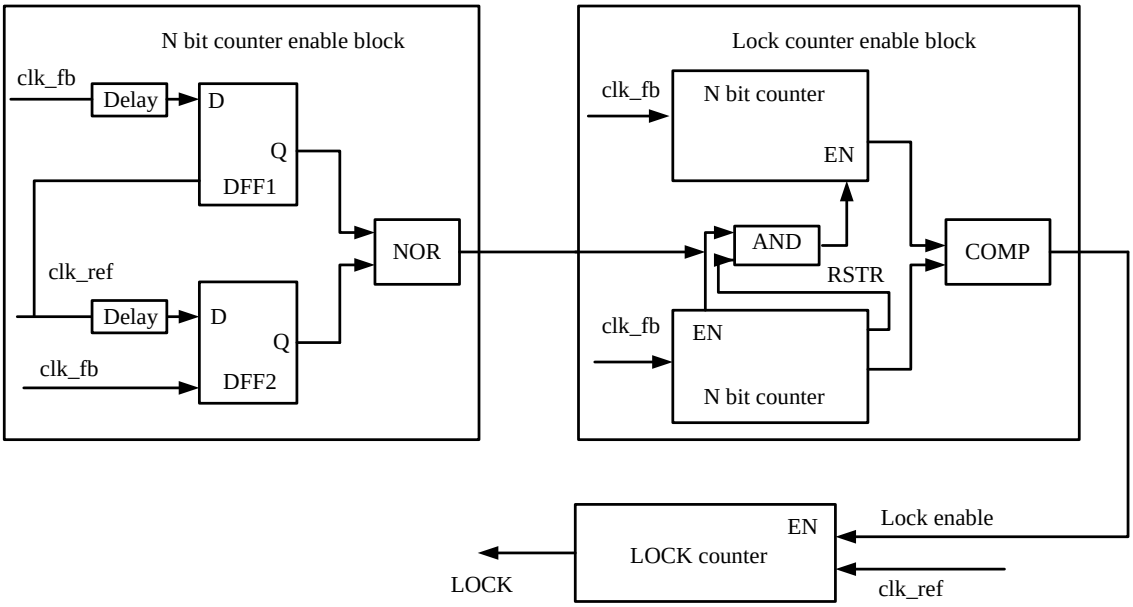

FIGURE 1. Digital lock detector

In fig 1, in the N-bit counter enable block there are two signals which are feedback and the reference signal. In [2] There are two delay elements to each of the D flip flop. The output of this block is high only if the both of the flip flops output is low. Now assume the case of this signal being high and passed to the lock counter enable block. As you can observe from the lock counter enable block from the fig 1, there are two N-bit counters which calculate the no. of high going pulses of feedback and the reference signal respectively.

The value of the N is predetermined according to the need. The value of the counters is then passed to the comparator block. It is to be noted that the value of the first counter is complimented and then passed to the comparator. This is done cause of internally the comparator is adder. So, the comparator actually performs the addition of a complemented signal and output of the other counter.

If this value is zero, it indicates that the values of both the counters is same which implies that the frequency of the reference signal and the frequency of the feedback signal is same. Thus the locking condition is achieved. Further it acts as the enable signal to the lock counter.

The key point here is that, though the locking condition is established, the whole circuit still works even though the locking condition is achieved. Due to the presence of feedback the counters still count the no. of high going pulses

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 17874 - 17880
Received 25 April 2021; Accepted 08 May 2021.

which is quite unnecessary. These unnecessary further operations are over coming in the proposed methodology, which combines the gate clocking technology to the existing digital lock detector shown in the fig 1.

PLL (phase locked loop) is useful in wireless application, its basic operation is the ability to detect the difference of phase between the two signals. If phase error exists the PLL reduces it by using the control mechanism. PLL includes a VCO (voltage-controlled oscillator), low pass filter and a phase detector.

The phase detector produces a voltage known as “error” voltage by comparing phases of the 2 signals. Low pass filter denies any higher frequencies other than the requirement of the filter. In this circuit we use dual loop PLL which contains fine tuning and coarse tuning, the dual loop is used for increased precision and control stability.

The D flip flop which is also known as delay flip flop or data flip flop has a clock signal so that it can change its states which is not present in the regular D type latch. The gated D flip flop is preferred over normal D flip flop in our circuitry which are DFF1 and DFF2. The D flip flop has data and control clock as their inputs and Q as output of the flip flop. The truth table of D flip flop is given in the table 1.

Table 1. Truth table of D flip flop

Control Clock	Data	Q	Next state (Qbar)
0	0	Q	Qbar
0	1	Q	Qbar
1	0	0	1
1	1	1	0

Proposed Methodology

A digital lock detector is used in between the two-phase locked loops of a dual phase locked loop, when the first phase locked loop detects the match of the input and the feedback signal. This digital lock detector locks this particular frequency and further sends it to the second PLL. The second PLL only used to filter off the unnecessary frequencies and lock it more accurately with incoming and the feedback signal.

The comparator block shown in the figure 1 is actually an adder. Internally it adds the feedback signal and the 2’s complement of the received signal. When these two signals are added if the output is non zero then it indicates that the both signals are not same and when the output is zero it indicates that the received signal and the feedback signal are the same. Which implies the locking condition is established and this information is further carried to the lock enable block as shown in the figure 1.

As discussed earlier, the issue in above mentioned circuit is that once the locking condition is established, the counter and the rest of the circuit still operate which is not necessary. This issue is over coming by the following design shown in fig 2.

A digital lock detector is used in between the two-phase locked loops of a dual phase locked loop, when the first phase locked loop detects the match of the input and the feedback signal. This digital lock detector locks this particular frequency and further sends it to the second PLL. The second PLL only used to filter off the unnecessary frequencies and lock it more accurately with incoming and the feedback signal.

The comparator block shown in the figure 1 is actually an adder. Internally it adds the feedback signal and the 2’s complement of the received signal. When these two signals are added if the output is non zero then it indicates that the both signals are not same and when the output is zero it indicates that the received signal and the feedback signal

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 17874 - 17880
Received 25 April 2021; Accepted 08 May 2021.

are the same. Which implies the locking condition is established and this information is further carried to the lock enable block as shown in the figure 1.

As discussed earlier, the issue in above mentioned circuit is that once the locking condition is established, the counter and the rest of the circuit still operate which is not necessary. This issue is over coming by the following design shown in fig 2.

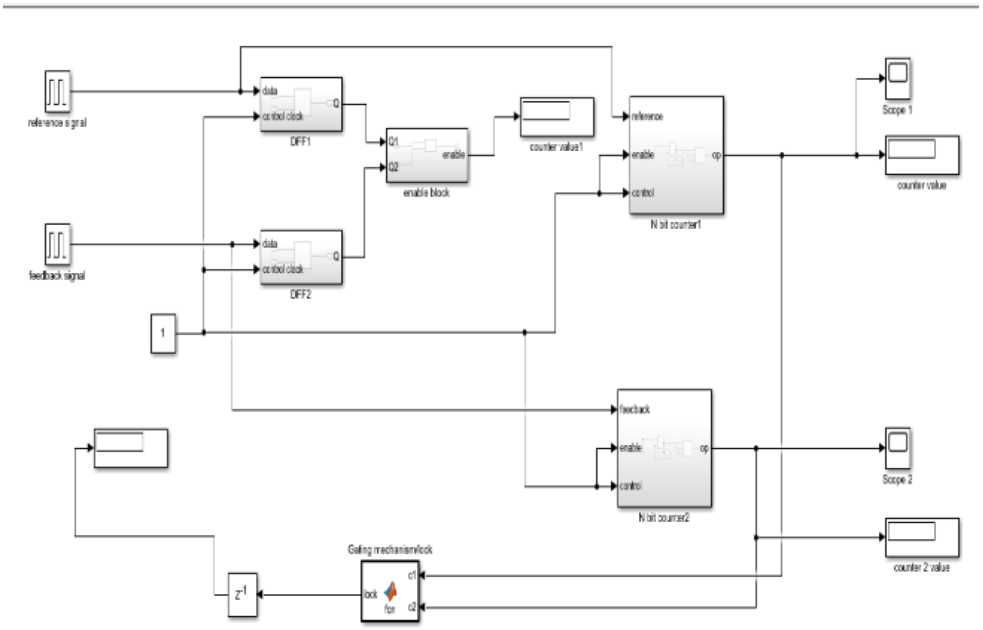

Figure 2. Proposed circuit design.

As shown in the figure 2, the proposed design is implemented in MATLAB Simulink software. First the existing circuit that is, fig 1 is implemented. Then the additional feature of locking mechanism block is introduced.

The fig 2 consists of two signal sources reference and feedback, two D flip flops, an enable block, two N-bit counters, Gate locking mechanism block and output display units. The whole operation is same as explained earlier in existing methodology of digital lock detector. The only difference is the inclusion of the gating block. What it does is that, once the counter values are reached to its predetermined values, the gate locking block stops the further operation of the counters and the rest of the circuit. This decreases the signal activity in the output and also saves dynamic power consumed internally.

Controller is an important area of the design in consideration. The input of the frequency divider is controlled by it and fault detector produces a signal by which a decision is decided by. If an input signal is free from fault, then output wave is made from the frequency divider with the data which is updated or else the output is made from previously obtained data from the circuit. Length of the reference signal is obtained from the finite state response. The DCO cycles determines the period of the given input reference signal. Frequency divider circuit is loaded with this value into it. State machine has t states and they are, start, reference high and reference low.

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 17874 - 17880
Received 25 April 2021; Accepted 08 May 2021.

Results

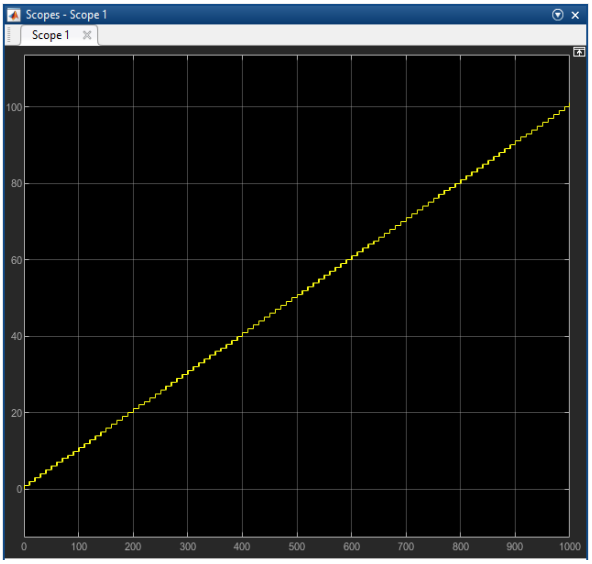

Figure 3. Counter o/p without gating method

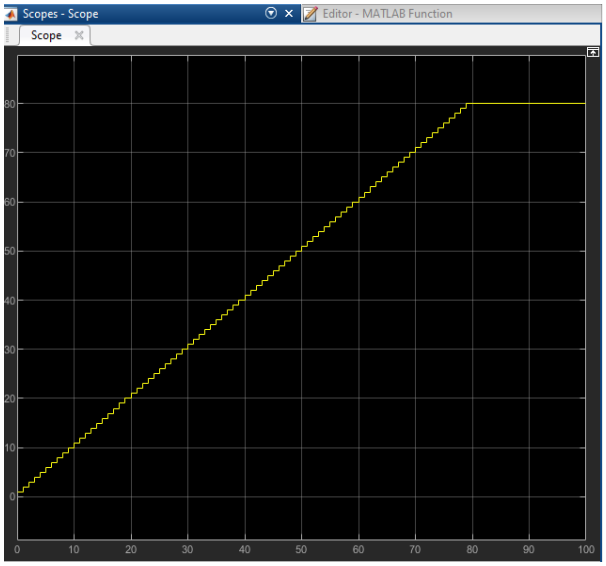

Figure 4. Counter o/p with Gating method

In figure 3, it is the scope output of the of the counter when gating mechanism block is deactivated and on the other side, the figure 4 represents the scope output of the counter when gating mechanism is activated. Consider the case when the counter value was set to 80. That is, we say that the two signals are locked if they reach to a count of 80 pulses at a predetermined time. As there is no gating mechanism, even after the counter reached its value, it still counts the pulses as there is no governing action or circuit to stop it. This governing circuit is introduced by the Gate clocking mechanism block.

Table 2. Power variance with no. of Pulses

S No.	Δ in No. of pulses	Δ in Dynamic power (watts)
1	10	4.295mW
2	20	12.314mW
3	30	16.214mW
4	40	18.044mW

In table 2, the power variance with the change in the no. of pulses is shown. This variation in no. of pulses is due to the introduction of the gating mechanism. The power is calculated from the power measurement block in slimscape library in MATLAB Simulink. For the calculation of the power, power supply with 1V V_{DD} with 1.4A current is used at an operation frequency of 375 MHz frequency.

As the paper title suggests, this circuit is a low power digital lock detector. Now this low power characteristic feature is achieved by decreasing dynamic power the output signal power of the digital lock detector. Dynamic power is given by the formula $P_{dynamic} = \alpha C_L V_{dd}^2 f$. In the above equation the variable α is a constant and is known as the switching activity coefficient and it depends on how often the 1's and 0's change in the signal and C_L is the load constant, which is the capacitance load of the entire circuit.

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 17874 - 17880
Received 25 April 2021; Accepted 08 May 2021.

$V_{dd}$is the voltage supply of the circuit which is fixed and is constant for the voltage which is fixed for this circuit. Also, f is the frequency of operation of the circuit. As mentioned above, it is said that the power of the output signal is calculate from the existing power calculation block defined in the MATLAB library.

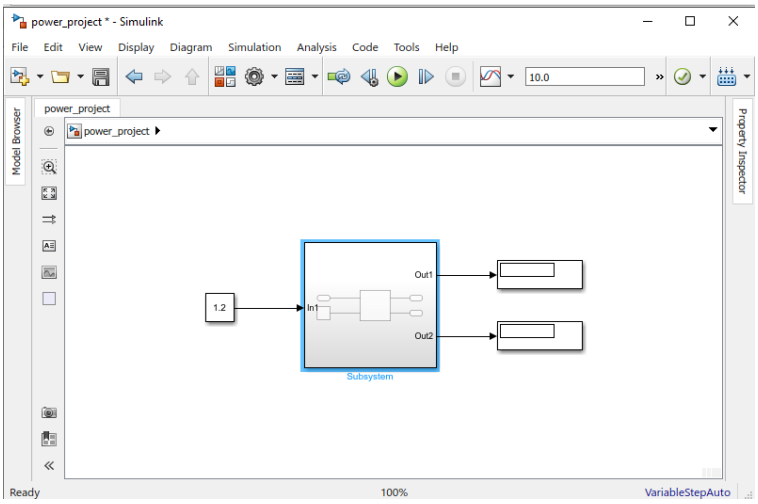

Figure 5. Simulink photo of power block.

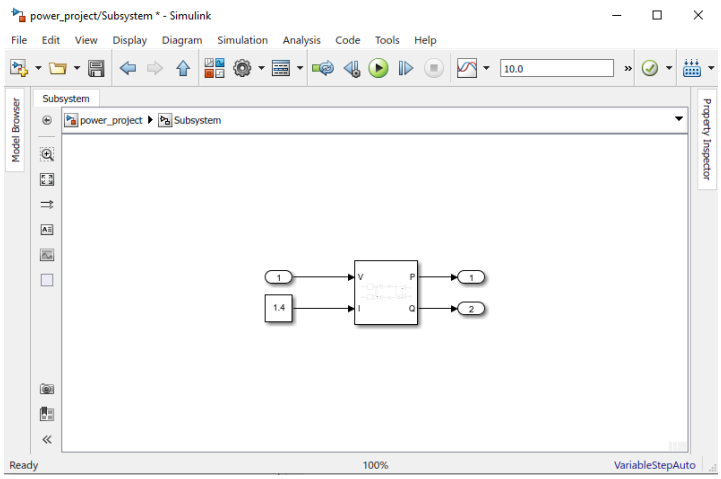

Figure 6. Simulink photo of subsystem in power

In the figure 5, we used the constant 1.2 as voltage and 1.4 as the current value in ampere in order to calculate the power. Table 1 depicts this power values for the various signals.

Conclusion

In this paper a low power digital lock detector with the additional feature of Gate clocking methodology is implemented in MATLAB SIMULINK software. Here the variance in the dynamic power due to introduction of gating mechanism is observed. This gating circuit can be further applied to other parts of the neighboring circuit. This optimized version of digital lock detector which uses gate clocking technique for D flip flop is best suited than that of normal D flip flop. Thus, this can be further investigated and has a lot of potential in it for further study.

Annals of R.S.C.B., ISSN:1583-6258, Vol. 25, Issue 6, 2021, Pages. 17874 - 17880
Received 25 April 2021; Accepted 08 May 2021.

Acknowledgement

We would like to thank our college management, principal and special mention to our HOD and supervisor. Without their help we wouldn't have done this work.

References

[1] Aparna B, Anandi V. Design of a D flip flop for optimization of power dissipation using GDI technique. In2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT) 2017 May 19 (pp. 172-177). IEEE.

[2] Bae CH, Yoo C. A digital lock detector for a dual loop PLL. In2014 International SoC Design Conference (ISOCC) 2014 Nov 3 (pp. 194-195). IEEE.

[3] V. Melikyan, A. Hovsepyan, M. Ishkhanyan and T. Hakobyan, "Digital lock detector for PLL," Design & Test Symposium (EWDTS), 2008 East-West, pp. 141-142, Oct 2008.

[4] Ming-ta Hsieh and Gerald E. Sobelman, "Architectures for Multi-Gigabit wire-linked clock and data recovery," Circuits and Systems Magazine, IEEE, vol. 8, issue 4, pp. 45-57, Fourth Quarter 2008.

[5] Shao-Ku Kao, Bo-Jiun Chen, and Shen-Iuan Liu, "A 62.5-625-MHz anti-Reset all-digital delay-locked loop", Circuits and Systems 11: Express Briefs, IEEE Transactions vol 54, issue 7, pp.566-570, July 2007.

[6] Yue-Fang Kuo, Ro-Min Weng, and Chuan-Yu Liu, "A fast locking PLL with phase error detector", Electron Devices and Solid-State Circuits, 2005 iEEE Conference, pp. 423-426, Dec. 2005.

[7] K. H. Cheng, W. B. Yang, and C. M. Ying, "A dual-slope phase frequency detector and charge pump architecture to achieve fast locking of phase-locked loop," IEEE Trans. Circuit and System 11, vol. 50, pp. 892-896, Nov 2003.