Annals of R.S.C.B., ISSN: 1583-6258, Vol. 25, Issue 5, 2021, Pages. 5844 - 5852
Received 20 May 2021; Accepted 25 May 2021.

A PTL based power efficient ALU block using 45nm Technology

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ABSTRACT

Pass Transistor Logic is one of the best among the available methods to implement circuits where low power plays a major role. This logic nullifies the leakage power in total power consumed by the circuit. This paper deals with the design of 4-Bit ALU. The proposed ALU is capable of performing AND, OR, XNOR, XOR, Sum, Carry operations of two 4-Bit binary numbers. A 4-Bit adder is designed by cascading Half-adder and Full-adder circuits to obtain sum, carry. For the purpose of selecting the desired operation 8:1 Multiplexers are used. The simulation result consists of power calculated for 4-Bit ALU,1-Bit Logical Block, Multiplexers. For the simulation of the circuits we have used virtuoso platform of Cadence tool with 45nm CMOS technology and supply voltage of 1V.

Keywords
Pass transistor; Arithmetic Logic Unit (ALU); Multiplexer (MUX); Full adder; Half adder.

Introduction

An Arithmetic and Logic Unit (ALU) is a digital circuit which is capable of performing arithmetic and logical operations. The arithmetic operations of ALU includes addition, subtraction, multiplication whereas logical operations are AND, OR, XNOR, XOR. The fundamental block of an ALU is adder. If we can able to reduce the power consumed by full adder we can bring down the amount of power consumed by ALU. In this research work 4-Bit ALU has been proposed. The paper is sorted as follows: Section II previous work, Section III deals with Pass Transistor logic (PTL), Section IV deals with design of 4- Bit ALU, followed by Simulation Results, Conclusion and References.

Previous Work

In G.Karthik Reddy[1] 1-Bit ALU using pass transistor logic design is proposed as shown in Fig.1.ALU circuit involves a Full adder which is designed using pass transistor logic based on multiplexers. The circuits are simulated using CMOS technology of 65nm with supply voltage, frequency values of 1.2V and 100 MHz respectively.

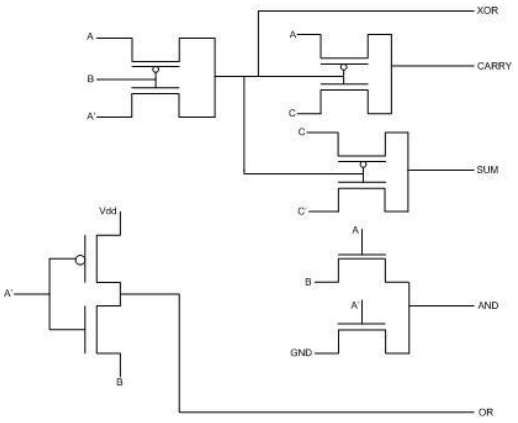

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Figure 1. 1-bit ALU using 10T

A 6T Full-adder circuit is designed using dual rail inputs as shown in Fig.2.The existing ALU is capable of generating Sum, Carry, XOR, AND, OR. The equations of sum, carry of full adder are modified as shown below.

$$sum = (a \oplus b) \oplus c$$
$$= (a \oplus b)c' + (a \oplus b)' c$$

$$carry = ab + bc + ca$$
$$= (a \oplus b)' a + (a \oplus b) c$$

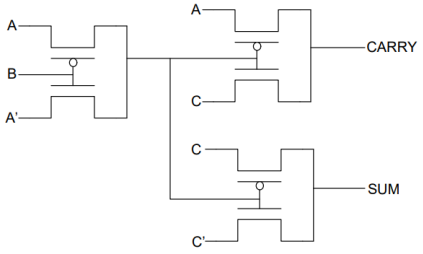

Figure 2. Full adder design using 6T

Pass Transistor Logic

PTL is one of the techniques to nullify the leakage power. Even though there are many techniques to reduce leakage power the following characteristics makes the difference between PTL and other methods.

• Length and Width of each transistor can be controlled which eliminates the glitches there by reducing the switching activity.

• In PTL Switching capacitance of a node is less when compared to a node in the conventional design i.e., CMOS design.

• The length and width of the transistor should be as small as possible in order to reduce the voltage drop across the transistor.

• The short circuit power is very low since the number of VDD to GND connections is very less. As there is no direct path from VDD to GND this makes sure that there is no static leakage.[2]

Design of 4-Bit ALU

In this work we have proposed a 4-Bit ALU as shown in Fig.3. The circuit of 4-Bit ALU comprises of four 1-Bit Logical Blocks, four blocks of 8:1 MUX and a 4-Bit ADDER. This ALU circuit is used to perform arithmetic and logical operations between two 4-Bit binary numbers. The inputs to the ALU block are A3-A0, B3-B0 where A3, B3 are MSB bits and A0, B0 are LSB bits.[3] These inputs are given to 1-Bit Logical Block and 4-Bit ADDER block. 1-Bit Logical Block performs AND, OR, XNOR, XOR logical operations and 4-Bit ADDER performs addition operation. 8:1 multiplexer is used to select the operation to be performed. The selected lines S0, S1, S2 are used to select the operations. Inputs for the multiplexer blocks are the outputs of 1-Bit ALU and adder blocks. The multiplexer has pins from D0 to D10 to extend the number of operations for future purpose. The outputs of the multiplexers are the final outputs of ALU block where OB0 is the LSB bit and OB3 is MSB bit.[4]

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Table 1. Truth Table of 8:1 Multiplexer

S0	S1	S2	OUTPUT
0	0	0	AND
0	0	1	OR
0	1	0	XOR
0	1	1	XNOR
1	0	0	ADDITION
1	0	1	-
1	1	0	-
1	1	1	-

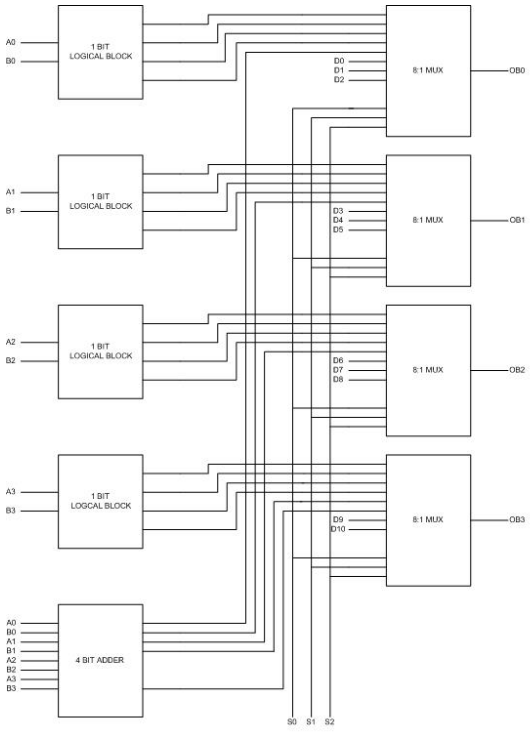

Figure 3. 4-Bit ALU

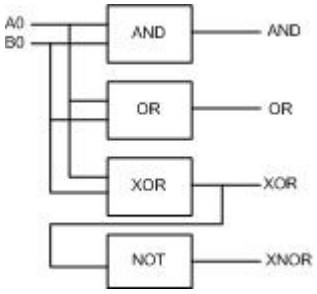

Figure 4. 1-Bit Logical Block

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1-Bit Logical Block which is shown in Fig.4 consists of blocks such as AND, OR, XNOR, XOR. Each block is design with Pass Transistor Logic with least number of transistors.

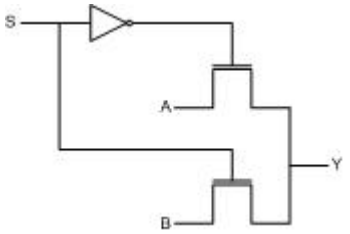

Figure 5. 2:1 multiplexer

Fig.5 shows the circuit of 2:1 Multiplexer. 8:1 Multiplexer is designed using 2:1 Multiplexers as shown in Fig.6[5] . A total of seven 2:1 multiplexers are cascaded to form a 8:1 multiplexer whereas 2: 1 multiplexer is designed using pass transistor logic.

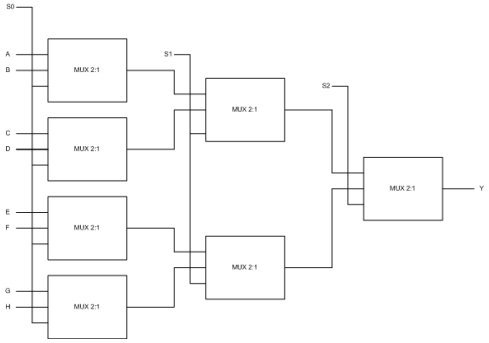

Figure 6. 8:1 Multiplexer using 2:1 multiplexer

The truth table mentioned in table 1 is for the first 3 8:1 multiplexers in 4-Bit ALU.
4-Bit adder is designed using half adder and full adder blocks[7] as shown in Fig.7 .

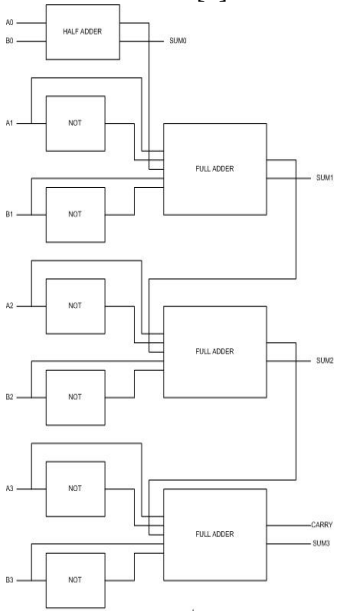

Figure 7.4-Bit Adder

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The carry which is generated in lowest significant bit is moving as input to the other significant bits of it, [6]by using full adder we can get the output of sum and carry of the next significant bits.

Simulation Results

Schematic Results

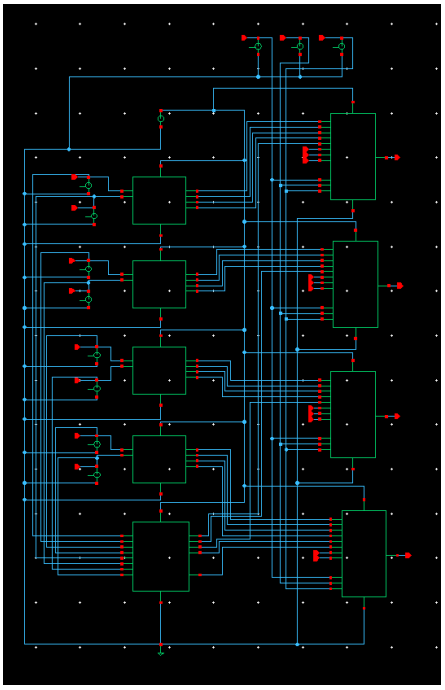

Figure 8. 4-Bit ALU

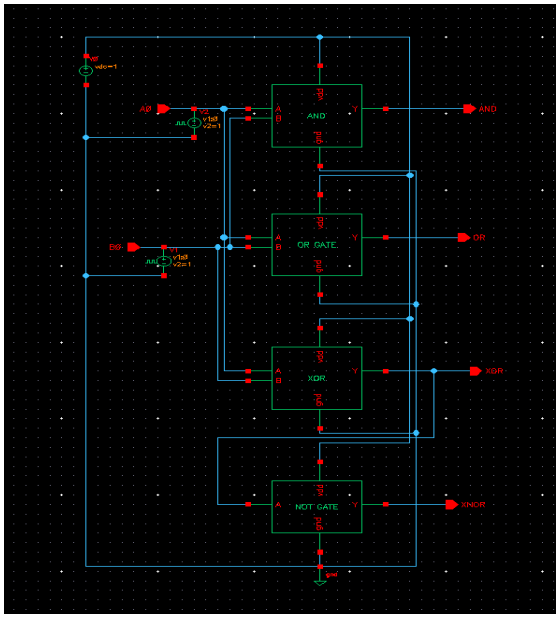

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Figure 9. 1-Bit Logical Block

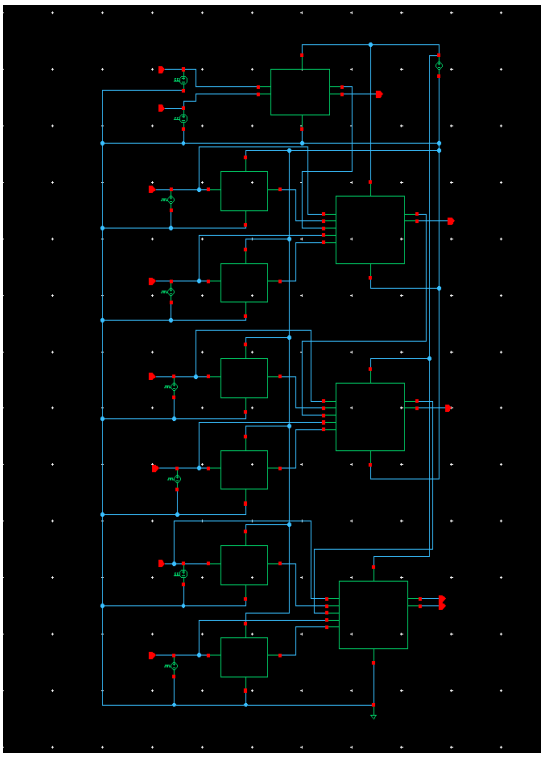

Figure 10. 4-Bit Adder

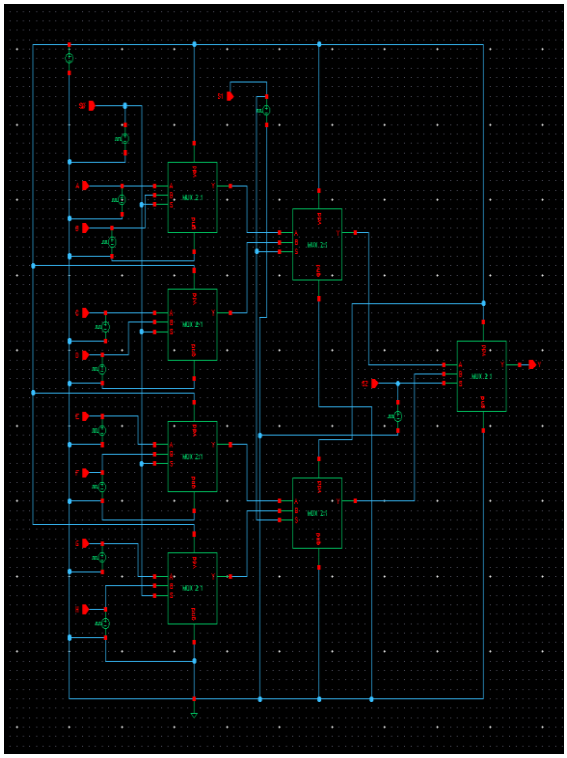

Figure 11. 8:1 Multiplexer

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Results

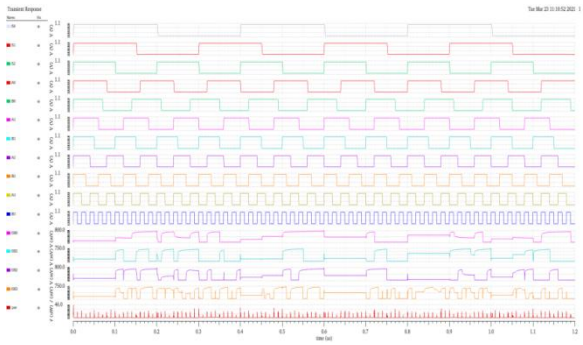

Figure 12. Transient response of 4-Bit ALU

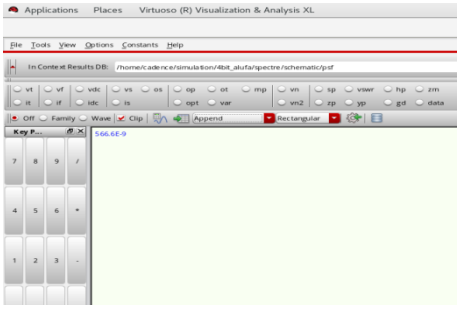

Figure 13. Power analysis of 4-Bit ALU

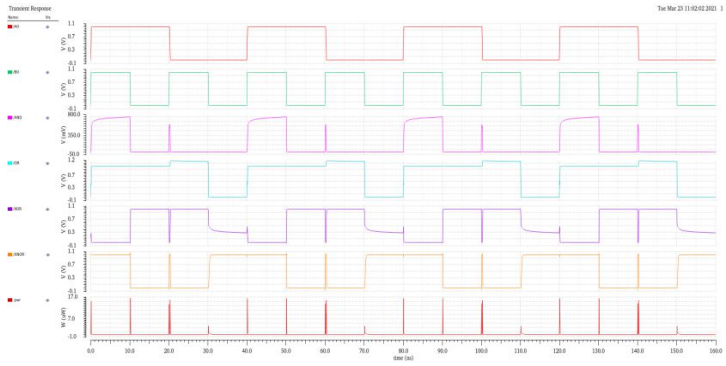

Figure 14. Transient response of 1-Bit Logical Block

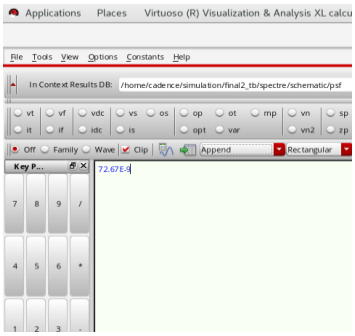

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Figure 15. Power analysis of 1-Bit Logical Block

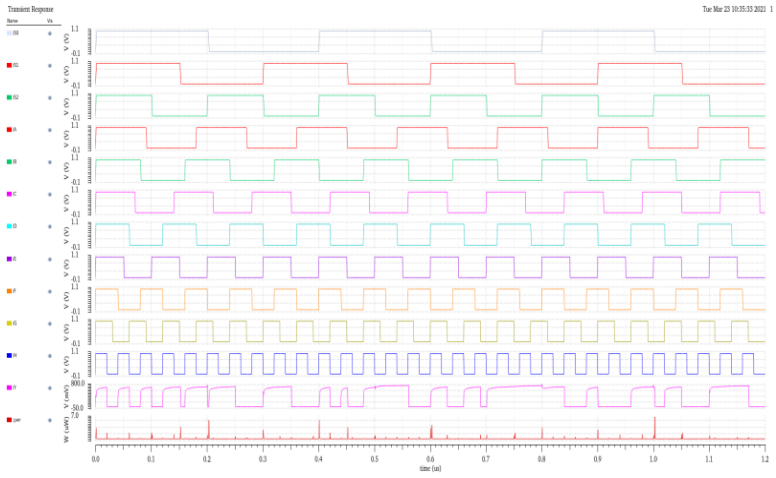

Figure 16. Transient response of 8:1 Multiplexer

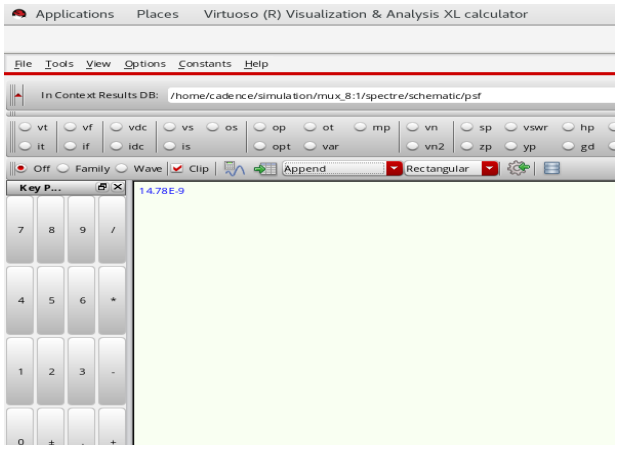

Figure 17. Power analysis of 8:1 Multiplexer

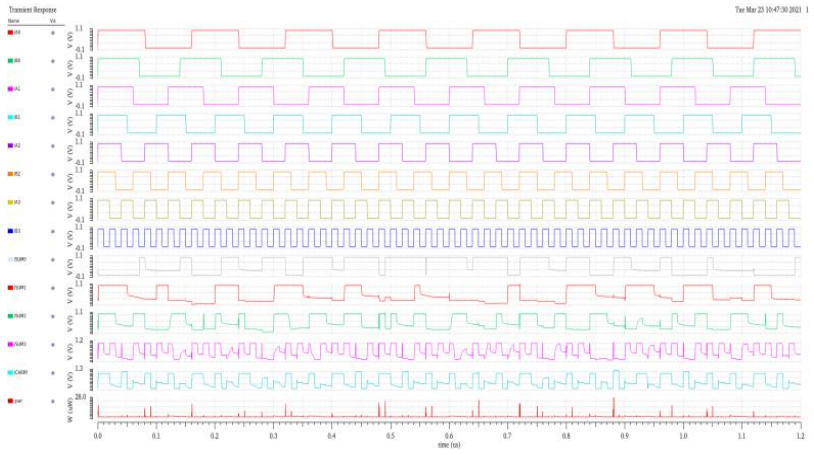

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Figure 18. Transient response of 4-Bit Adder

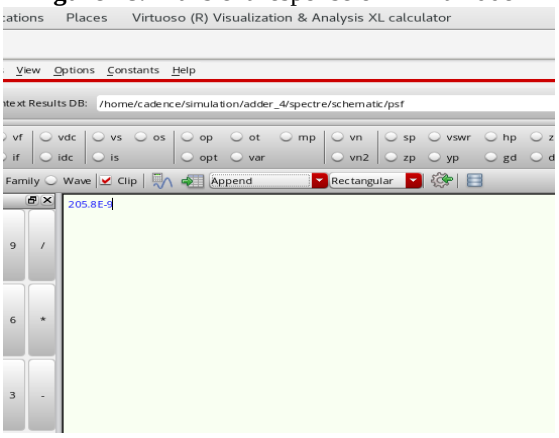

Figure 19. Power analysis of 4-Bit Adder

Conclusion

In this work, we have designed a 4-Bit ALU.1-Bit Logical Block, Multiplexers, 4-Bit Adder circuits are cascaded to acquire a 4-Bit ALU. Pass Transistor Logic .relatively uses less number of transistors compared to the conventional method of designing a circuit and also it reduces the leakage power. So this ALU works efficiently for applications where Low Power is preferred.

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